



M13design

M13-RA6M3-EK

**RA6M3 (Cortex-M4)
Evaluation Kit**

USER MANUAL

TABLE OF CONTENT

1	OVERVIEW	7
1.1	Introduction	7
1.2	Features	8
2	HARDWARE LAYOUT AND CONFIGURATION.....	9
2.1	Hardware block diagram	9
2.2	The M13-RA6M3-EK Board layout	10
3	M13-RA6M3-EK PIN ASSIGNMENT.....	12
3.1	RA6M3 system and Power pins.....	12
3.1.1	Boot pin.....	12
3.1.2	System Reset pin.....	12
3.1.3	Clock source	13
3.1.4	Power supply	14
3.2	External memory	15
3.2.1	Serial Flash Memory	15
3.2.2	SDRAM	16
3.2.3	EEPROM	17
3.3	4.3-inch TFT LCD Module	18
3.4	USB Interface	19
3.5	LAN Interface	20
3.6	SD/MMC Host Interface (4-bits).....	21
3.7	Audio Interface	22
3.8	3-Axis Accelerometer	23
3.9	J-Link OB.....	24
3.10	VGA camera module	26
3.11	I ² C Interface	27
3.12	User Interface: Switch, Led, Potentiometer	28
4	CONNECTOR OVERVIEW.....	29
4.1	CN1: USB-Micro A/B	29
4.2	CN2: USB-Micro A/B	29
4.3	CN4: 19-Pin JTAG Header.....	30
4.4	CN6: RJ45.....	31
4.5	CN7: LCD Connector	32
4.6	CN8: LCD Capacitive Touch	33
4.7	CN9: 8 Bit VGA Camera module	33
4.8	CN10: Micro SD Card	34
4.9	CN11: 4-Pole Audio Jack	35
4.10	CN12: Expansion Connector - mikroBUS	36
4.11	CN13/CN14: Expansion Connectors – PMOD.....	37
4.12	CN15: +5VDC Power Jack.....	39

TABLE OF CONTENT (Continued)

5	MULTIPLEXED FUNCTIONS.....	40
5.1	SDRAM Selection	41
5.1.1	DATA / SPI0.....	42
5.1.2	ADDR / SSIE0.....	42
5.1.3	ADDR / SCI2.....	42
5.1.4	ADDR / SCI6.....	43
5.1.5	PMOD2	43
5.1.6	“Default” and “SDRAM ready” shunt Configuration recap	44
5.2	SD CARD / QSPI	45
5.3	TDI / CTS2 / IRQ11.....	46
5.4	SDA0_B / USB_VBUS	47
6	RELATED DOCUMENTS	48
7	ORDERING INFORMATION.....	49
8	TECHNOLOGY PARTNERS	50
9	REVISION HISTORY	51

LIST OF TABLES

Table 1. Top main component list	11
Table 2. Bottom main component list	11
Table 3. Boot pins.....	12
Table 4. JP2	12
Table 5. System Reset pin	12
Table 6. Clock Source Assignment	13
Table 7. Serial Flash Memory Overview	15
Table 8. Serial Flash Memory Pin Assignment	15
Table 9. SDRAM overview	16
Table 10. SDRAM Address Bus Pin Assignment.....	16
Table 11. EEPROM Overview.....	17
Table 12. IIC0 Pin assignment	17
Table 13. TFT LCD Module Overview.....	18
Table 14. Capacitive Touchscreen	18
Table 15. LCD Assignment Pins	18
Table 16. USB Overview	19
Table 17. USB Pin Assignment.....	19
Table 18. Ethernet PHY Overview	20
Table 19. Ethernet Assignment Pins	20
Table 20. P706 Multiplexing	20
Table 21. SD/MMC Interface Pin Assignment.....	21
Table 22. Audio CODEC Overview	22
Table 23. Audio Pin Assignment	22
Table 24. Accelerometer Overview	23
Table 25. IIC0 Pin assignment	23
Table 26. SWD/JTAG Pin Assignment.....	24
Table 27. Debug Configuration.....	25
Table 28. VGA Camera Module Overview	26
Table 29. 8bit VGA Interface Pin Assignment.....	26
Table 30. I ² C pin assignment.....	27
Table 31. User Interface Overview.....	28
Table 32. User Interface Pin Assignment.....	28
Table 33. CN1 Pin Description	29
Table 34. CN2 Pin Description	29
Table 35. CN4 Pin Assignment	30
Table 36. CN6 Pin Assignment	31
Table 37. CN7 Pin Assignment	32
Table 38. CN8 Pin Assignment	33
Table 39. CN9 Pin Assignment	33

LIST OF TABLES (Continued)

Table 40. CN10: Micro SD Card Pin Assignment.....	34
Table 41. CN11 Pin Assignment	35
Table 42. CN12 Pin Assignment	36
Table 43. mikroBUS™ Overview	36
Table 44. PMOD Connector Overview	37
Table 45. CN13 (PMOD1) Pin Assignment	37
Table 46. CN14 (PMOD2) Pin Assignment.....	38
Table 47. CN15 Connector Overview.....	39
Table 48. CN15 Pin Assignment	39
Table 49. Multiplexing Function Table.....	40
Table 50. Multiplexing SDRAM Data & SPI0.....	42
Table 51. Multiplexing SDRAM Addresses & SSIE0.....	42
Table 52. Multiplexing SDRAM Addresses & SCI2.....	42
Table 53. Multiplexing SC6 & SDRAM Addresses.....	43
Table 54. Multiplexing PMOD_RST & SDRAM Address.....	43
Table 55. Shunt Configuration.....	44
Table 56. QSPI/SDHI Selection	45
Table 57. Multiplexing TDI / CTS2 / IRQ11	46
Table 58. Multiplexing SDA0_B & USB_VBUS	47
Table 59. Ordering Information	49
Table 60. Default/SDRAM-Ready Features	49
Table 61. Hardware Technology Partners.....	50
Table 62. Software Technology Partners	50
Table 63. Revision Table	51

LIST OF FIGURES

Figure 1. M13-RA6M3-EK Component View (Top).....	7
Figure 2. M13-RA6M3-EK LCD View (Bottom)	7
Figure 3. Bloc Diagram.....	9
Figure 4. Top main component Layout.....	10
Figure 5. Bottom main component layout (Bottom view)	10
Figure 6. Reset Block Diagram.....	12
Figure 7. Clock Source Diagram	13
Figure 8. RA6M3 Power Supply Overview	14
Figure 9. USB Diagram	19
Figure 10.SD/MMC Host Interface Diagram.....	21
Figure 11. Audio Block Diagram.....	22
Figure 12. Debug Interface Diagram	24
Figure 13. SW2 Illustration	25
Figure 14. I ² C bus diagram.....	27
Figure 15. User Interface diagram.....	28
Figure 16. CN1: USB-Micro A/B Front view	29
Figure 17. CN2: USB- Micro A/B Front view	29
Figure 18. CN4: 19-pin JTAG Header	30
Figure 19. CN6. RJ45 Bottom View	31
Figure 20. CN7. Front View	32
Figure 21. CN8 Front View	33
Figure 22. CN9 Front View	33
Figure 23. CN10: MicroSD Card Bottom View	34
Figure 24. CN11 Mating Plug and Bottom View.....	35
Figure 25. CN12 mikroBUS™ Top view	36
Figure 26. PMOD Front View	37
Figure 27. CN15 Power Jack.....	39
Figure 28. Shunt Footprint.....	40
Figure 29. Shunt general location	41
Figure 30. JP3 to JP8 Top location	45

1 OVERVIEW

1.1 INTRODUCTION

The **M13-RA6M3-EK** is complete evaluation and development platform for the Renesas Electronics® 32-bit Microcontroller RA family Cortex®-M4 based R7FA6M3AH3CFC microcontroller. The full range of the hardware features on the board helps users to quickly evaluate all the available peripherals (10/100-Mbit Ethernet, microSD™ card, USB HS/FS, Audio codec with 4-pole Jack, SDRAM, Quad-SPI Flash memory, 4.3-inch colour LCD-TFT with capacitive touch panel, and many others) and to develop their custom applications. PMOD™ and Mikrobus™ connectors make it possible to easily extend the board's features (Sensors, communication and network modules and many more). The integrated JLink-OB debug probe provides in-circuit debug and programming for the RA6M3 device and also a built-in VCOM functionality.

Figure 1. M13-RA6M3-EK Component View (Top)

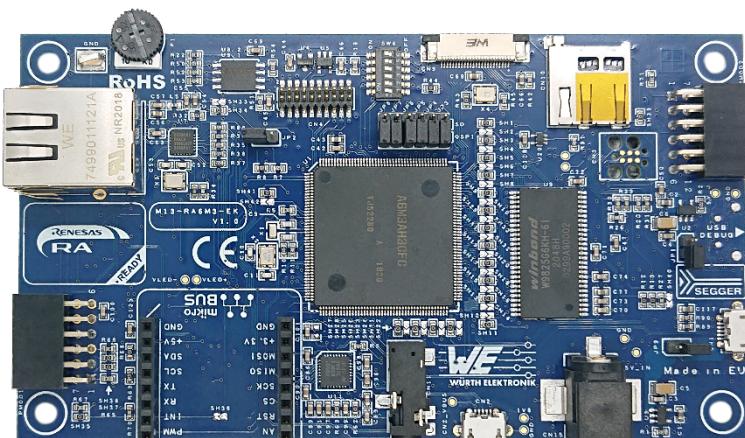
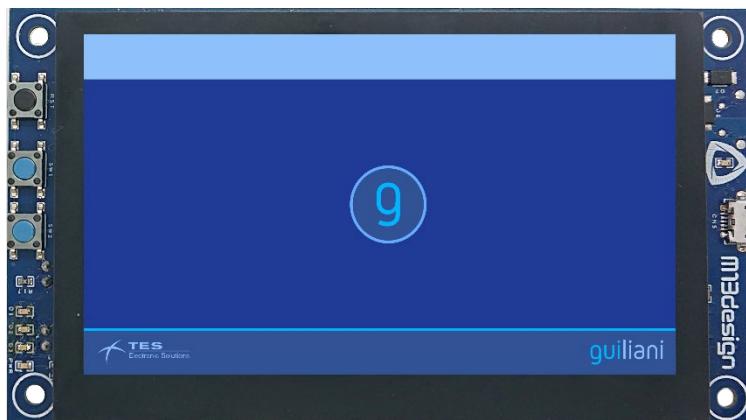


Figure 2. M13-RA6M3-EK LCD View (Bottom)

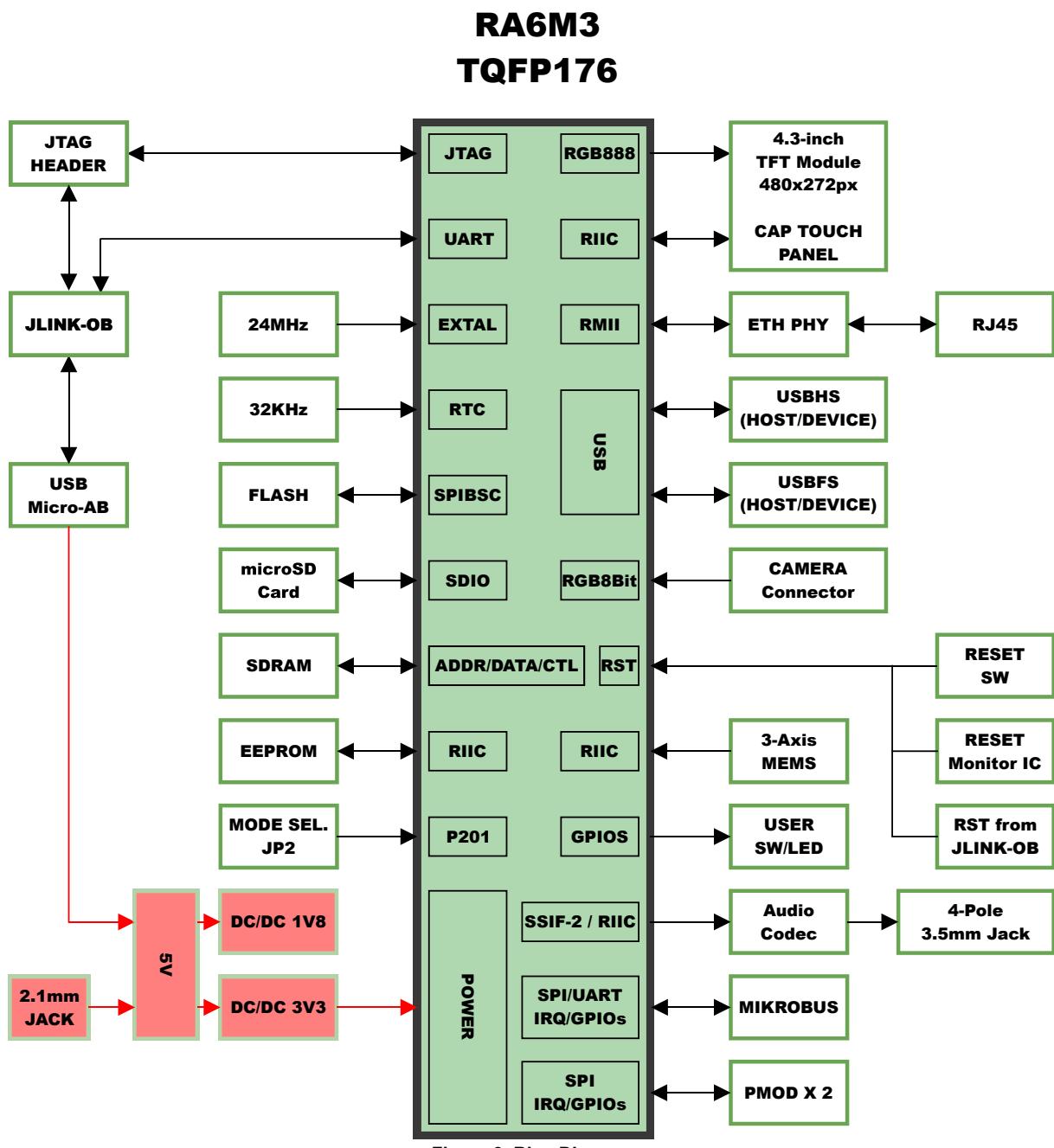


1.2 FEATURES

- Renesas RA6M3 (Cortex®-M4) Microcontroller R7FA6M3AH3CFC
- LQFP176 Package
- 2Mbyte Internal Flash
- 640Kbyte Internal RAM
- 32Mbyte external SDRAM (Multiplexed)
- 32Mbyte external Serial Flash
- 16Kbit I²C EEPROM
- 4.3-inch 480x272 TFT LCD with capacitive touch panel
- USB Interface
- LAN Interface
- SD/MMC Host Interface (4 bits)
- I2S Audio codec
- 3-Axis accelerometer
- On-board JLINK-OB debugger with VCOM
- 19-pins 1.27mm pitch JTAG connector
- Board connectors
 - 1 x 8-bit Interface camera
 - 1 x Ethernet RJ45
 - 2 x USB Micro-AB
 - 1 x USB Micro-AB for debugger
 - 1 x microSD™ card
 - 1 x Mikrobus™
 - 2 x PMOD
 - 1 x 4-pole 3.5mm Jack
 - 1 x 2.1mm 5V Power Jack
- 2 x User switch and 1 x Reset switch
- 1 x Mono-turn 10KΩ Potentiometer
- 3 x User LEDs
- 1 x Power-on LED

2 HARDWARE LAYOUT AND CONFIGURATION

2.1 HARDWARE BLOCK DIAGRAM



2.2 THE M13-RA6M3-EK BOARD LAYOUT

Figure 4 and **Figure 5** Show the layout of the main components of the board.

Figure 4. Top main component Layout

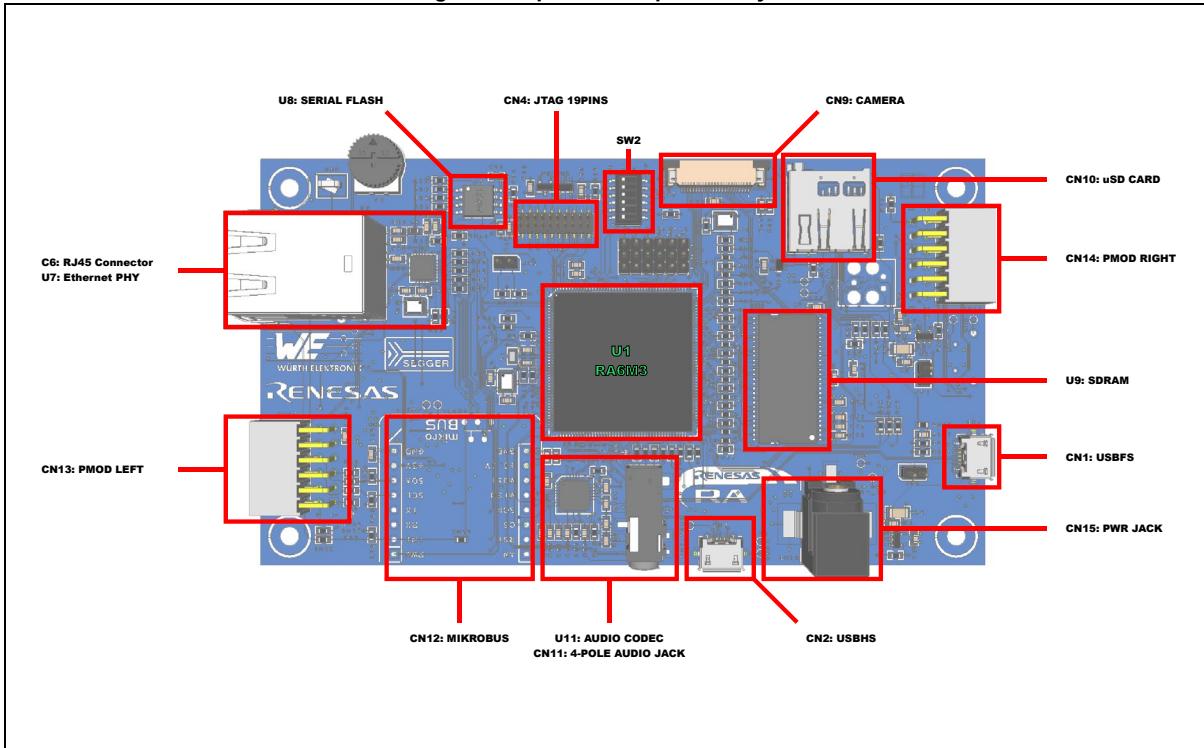


Figure 5. Bottom main component layout (Bottom view)

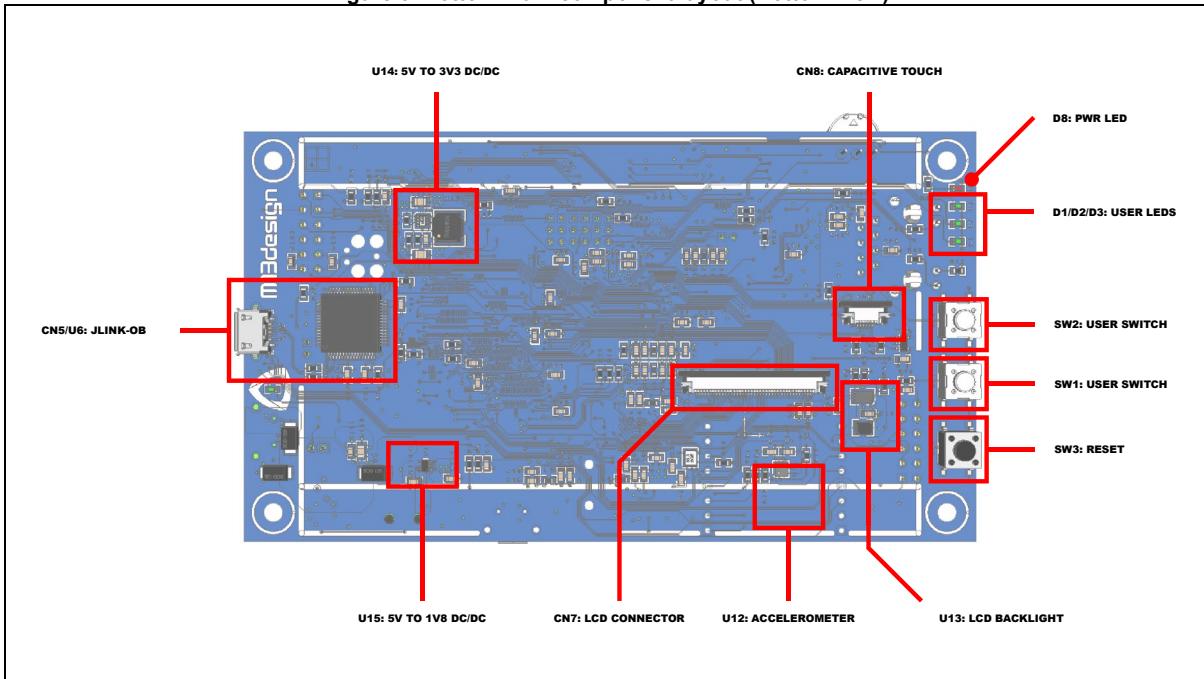


Table 1 And **Table 2** list the main component mounted on the M13-RA6M3-EK board

Table 1. Top main component list

Component Reference	Description	MFR ¹ / MPN ²	NOTES
U1	CPU	Renesas / R7FA6M3AH3CFC	
U7	Ethernet PHY	Microchip / KSZ8081RNA	
U8	Serial Flash Memory	Macronix / MX25L25645GM2I-08G	
U9	SDRAM	Winbond / W9825G6KH-6I	
U11	Audio Codec	Maxim / MAX9867ETJ	
CN1	USB FS	Würth Electronics / 629105150921	Mini USB-AB
CN2	USB HS	Würth Electronics / 629105150921	Mini USB-AB
CN4	19pins JTAG connector	Würth Electronics / 62102021021	1.27mm Pitch
CN6	RJ45 connector	Würth Electronics / 7499011121A	
CN9	Camera connector	Würth Electronics / 68712414022	Top contact
CN10	Micro SD Card	Würth Electronics / 693071010811	
CN11	4-pole Jack headphone	Cui Inc. / SJ-43514-SMT-TR	3.5mm
CN12	mikroBUST™	Würth Electronics / 61300811821	CN12.1 & CN12.2 in the BOM
CN13	PMOD1	Würth Electronics / 613012243121	
CN14	PMOD2	Würth Electronics / 613012243121	
CN15	5V, 2.1mm, Power Jack	Würth Electronics / 694106105102	Strictly 5VDC
SW2	JLink-OB Disconnection	Omron / A6H-6101	

Table 2. Bottom main component list

Component Reference	Description	MFR ¹ / MPN ²	NOTES
U6	JLink-OB	Segger	
U12	3-Axis Accelerometer	Würth Electronics / 2533020201601	
U13	LCD Backlight	Renesas / ISL97634IRT26Z-T	
U14	3V3 DC/DC regulator	Renesas / ISL80030AFRZ-T7A	
U15	1V8 DC/DC regulator	Renesas / ISL9008AIECZ-T	
CN5	JLink-OB connector	Würth Electronics / 629105150921	Mini USB-AB
CN7	LCD connector	Würth Electronics / 687140183722	Bottom contact
CN8	Capacitive Touch connector	Würth Electronics / 687106183722	
D1/D2/D3	User Leds	Würth Electronics / 150060VS55040	Green Led
D8	Power Led	Würth Electronics / 150060RS55040	Red Led
SW1	Reset Switch	C&K / PTS645SL43SMTR92LFS	Black coloured
SW3/SW4	User Switches	C&K / PTS645SM43SMTR92LFS	Blue coloured

Note 1: Manufacturer name

Note 2: Manufacturer Part Number

3 M13-RA6M3-EK PIN ASSIGNMENT

3.1 RA6M3 SYSTEM AND POWER PINS

3.1.1 BOOT PIN

Table 3. Boot pins

U1 Pin	Pin Functions	Board Assignment	Signal Name	Default Function	Remarks
68	P201/MD	MD	N/A	System	

By default, the board is in **Single-Chip mode** (JP2 left open). In order to switch to **SCI/USB boot mode**, connect JP2 with a 2mm jumper as stated in [Table 4](#).

Table 4. JP2

U1 Pin	Pin Functions	JP2	Pin status	Operating Mode
68	P201/MD	Opened	Pulled-up	Single-chip mode
68	P201/MD	Closed	Pulled-down	SCI/USB boot mode

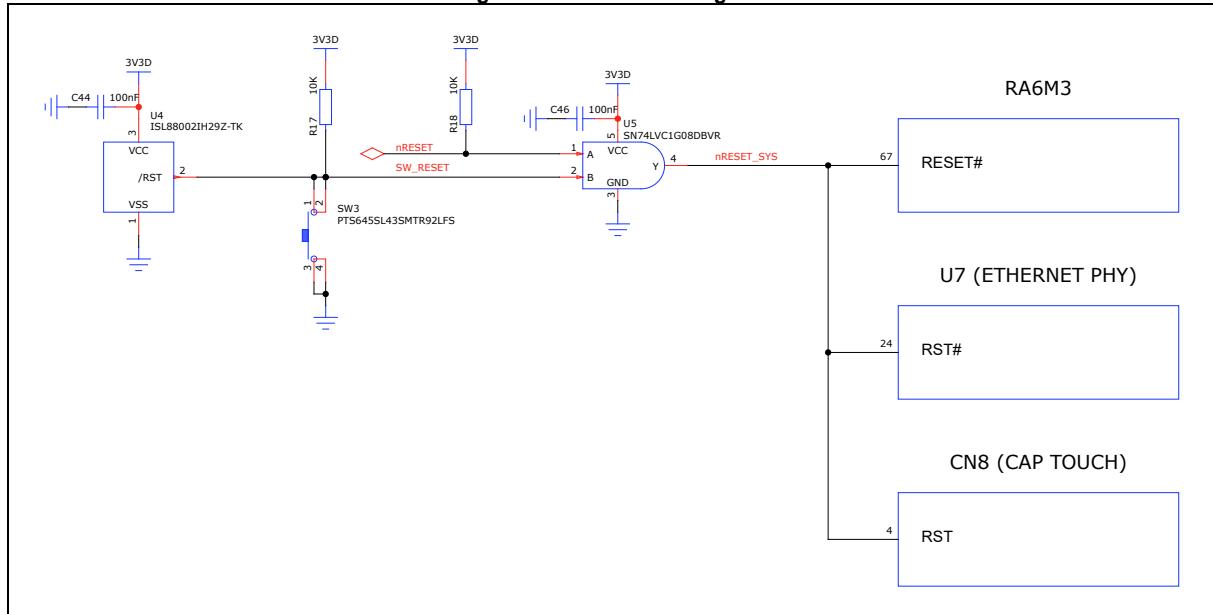
3.1.2 SYSTEM RESET PIN

Table 5. System Reset pin

U1 Pin	Pin Functions	Board Assignment	Signal Name	Default Function	Remarks
67	RESET#	Reset	nRESET_SYS	System	

The **M13-RA6M3-EK** System Reset signal is controlled by 3 sources: The power-on reset with the Voltage supervisor U4, the Reset Switch (SW1) and the JTAG reset signal. [Figure 6](#) shows the reset block diagram.

Figure 6. Reset Block Diagram



As illustrated in [Figure 6](#), the board's Reset signal is also directly connected to the Reset signal of the Ethernet PHY (U7) and the Capacitive Touch driver (CN8). This is done to compensate the lack of free GPIOs left after mapping all the dedicated peripheral of the board.

3.1.3 CLOCK SOURCE

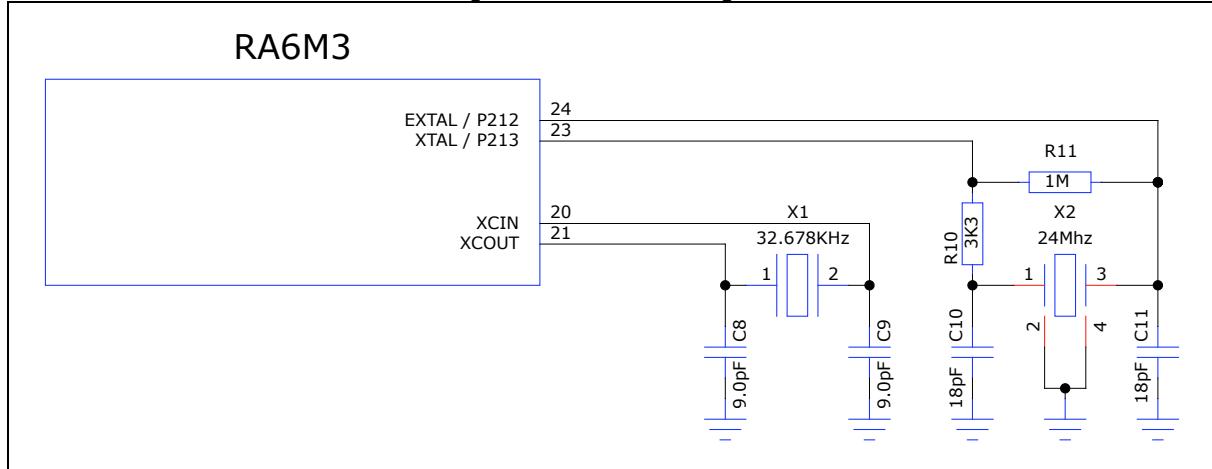
The **M13-RA6M3-EK** has 2 clock input sources as shown in [Figure 7](#) and [Table 6](#) gives you the connections for each clock on the RA6M3.

- Main clock : 24MHz crystal
- RTC clock : 32.768KHz crystal

Table 6. Clock Source Assignment

U1 Pin	RA6M3 Pin Functions	Board Function Assignment	Signal Name	Default Function	Remarks
24	EXTAL/P212	Main clock	EXTAL	Clock	
23	XTAL/P213	Main clock	XTAL	Clock	
20	XCIN	RTC clock	XCIN	Clock	
21	XCOUP	RTC clock	XCOUP	Clock	

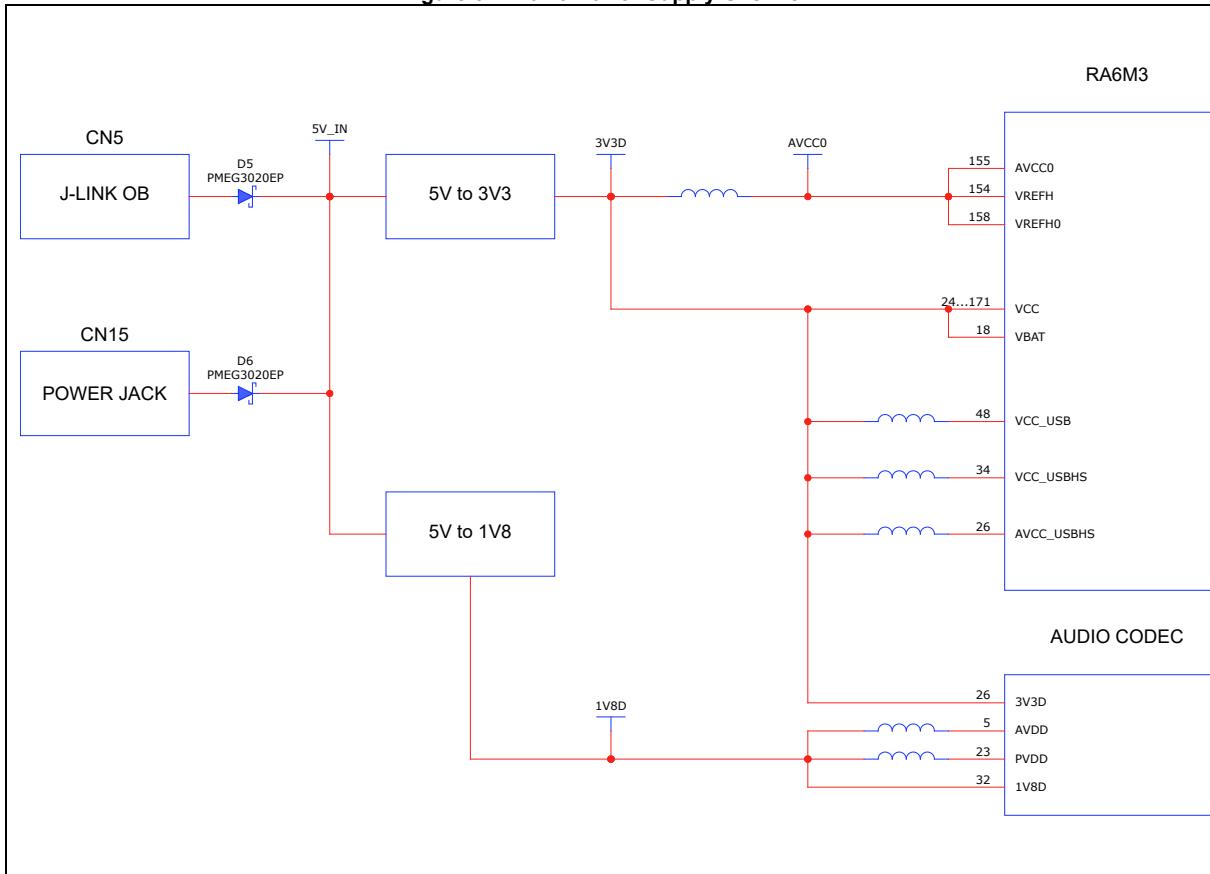
Figure 7. Clock Source Diagram



3.1.4 POWER SUPPLY

The **M13-RA6M3-EK** has 2 sources for its power supply. The Primary source is from the +5VDC/500mA of the J-Link OB USB connector CN5 as shown in [Figure 8](#). The Secondary source is provided through the 2.10mm Power Jack connector CN15 and is strictly limited to a +5VDC power supply. Even though the power source is protected by diodes (D5 and D6) be extra cautious as to not provide the board's power from the Primary and the Secondary sources simultaneously.

[Figure 8. RA6M3 Power Supply Overview](#)



Two DC/DC regulators are used to generate all the required power rails needed on the board. The 1V8 rail is exclusively used by the Audio Codec as shown by the [Figure 8](#).

3.2 EXTERNAL MEMORY

3.2.1 SERIAL FLASH MEMORY

The **M13-RA6M3-EK** board is equipped with a serial flash memory which is controlled by RA6M3 on-chip Quad Serial Peripheral Interface (QSPI). By default, the Serial Flash Memory is connected to the MCU but it can be switched to SD Card anytime. [Table 7](#) Shows the serial Flash Memory Overview.

Table 7. Serial Flash Memory Overview

Device Type	MFR ¹ / MPN ²	Operational Voltage	Capacity	Package
Serial Flash	Macronix / MX25L25645GM2I-08G	3.3V	32Mbyte	8-SOP (200mil)

Note 1: Manufacturer name

Note 2: Manufacturer Part Number

[Table 8](#) Shows the pin assignment between the RA6M3 CPU (U1) and the Serial Flash Memory (U8).

Table 8. Serial Flash Memory Pin Assignment

U1 Pin	RA6M3 Pin Functions	Board Assignment	Signal Name	Default Function	Remarks
140	P500	JP3	QSPCLK	QSPI	Multiplexed
141	P501	JP4	QSSL	QSPI	Multiplexed
142	P502	JP5	QIO0	QSPI	Multiplexed
143	P503	JP6	QIO1	QSPI	Multiplexed
144	P504	JP7	QIO2	QSPI	Multiplexed
145	P505	JP8	QIO3	QSPI	Multiplexed

The Serial Flash Memory device is connected to the RA6M3 through the JP3-JP8 jumpers. See Section [5.2 SD CARD](#) for detailed information on multiplexing the P500-P505 signals.

3.2.2 SDRAM

The **M13-RA6M3-EK** is also equipped with an external 16 bits SDRAM. This memory device is controlled by the RA6M3 Bus State Controller. [Table 9](#) shows the SDRAM Memory Overview while [Table 10](#) shows the pin assignment between the RA6M3 and the SDRAM device.

Table 9. SDRAM overview

Device Type	MFR ¹ / MPN ²	Operational Voltage	Capacity	Package
SDRAM	Winbond / W9825G6KH-6I	3.3V	32Mbyte	TSOP54

Note 1: Manufacturer name

Note 2: Manufacturer Part Number

Table 10. SDRAM Address Bus Pin Assignment

U1 Pin	RA6M3 Pin Functions	Board Assignment	Signal Name	Default Function	Remarks
96	P115 / SSITXD0_B / A01	Multiplexed	A1	SSIE0	
95	P114 / SSIRXD0_B / A02	Multiplexed	A2	SSIE0	
94	P113 / SSILRCK0 / A03	Multiplexed	A3	SSIE0	
93	P112 / SSIBCK0_B / A04	Multiplexed	A4	SSIE0	
92	P111 / IRQ4 / A05	Multiplexed	A5	PMOD2	
87	P301 / RXD2 / A06	Multiplexed	A6	MIKROBUS	
86	P302 / TXD2 / A07	Multiplexed	A7	MIKROBUS	
85	P303 / A08	SDRAM	A8	SDRAM	
82	P304 / SCL6 / A09	Multiplexed	A9	SCI6	
81	P305 / SD6 / A10	Multiplexed	A10	SCI6	
80	P306 / A11	SDRAM	A11	SDRAM	
79	P307 / A12	SDRAM	A12	SDRAM	
78	P308 / A13	SDRAM	A13	SDRAM	
77	P309 / A14	SDRAM	A14	SDRAM	
76	P310 / A15	SDRAM	A15	SDRAM	
132	P100 / MISOA_A / DQ0	Multiplexed	DQ0	SPI	
131	P101 / MOSIA_A / DQ1	Multiplexed	DQ1	SPI	
130	P102 / RSPCKA_A / DQ2	Multiplexed	DQ2	SPI	
129	P103 / SSLA0_A / DQ3	SDRAM	DQ3	SDRAM	
128	P104 / SSLA1_A / DQ4	Multiplexed	DQ4	PMOD1	
127	P105 / SSLA2_A / DQ5	Multiplexed	DQ5	PMOD2	
126	P106 / SSLA3_A / DQ6	SDRAM	DQ6	SDRAM	
125	P107 / DQ7	SDRAM	DQ7	SDRAM	
103	P612 / DQ8	SDRAM	DQ8	SDRAM	
104	P613 / DQ9	SDRAM	DQ9	SDRAM	
105	P614 / DQ10	SDRAM	DQ10	SDRAM	
117	P605 / DQ11	SDRAM	DQ11	SDRAM	
118	P604 / DQ12	SDRAM	DQ12	SDRAM	
119	P603 / DQ13	SDRAM	DQ13	SDRAM	
133	P800 / DQ14	SDRAM	DQ14	SDRAM	
134	P801 / DQ15	SDRAM	DQ15	SDRAM	
100	P609 / CKE	SDRAM	CKE	SDRAM	
99	P608 / A0 / DQM1	SDRAM	A00/DQM1	SDRAM	UDQM
121	P601 / DQM0	Multiplexed	DQM0	PMOD2	LDQM
75	P311 / RAS	SDRAM	RAS#	SDRAM	
102	P611 / SDCS#	SDRAM	SDCS#	SDRAM	
74	P312 / CAS	SDRAM	CAS#	SDRAM	
101	P610 / WE	SDRAM	WE#	SDRAM	

As detailed in the [Table 10](#), the SDRAM device U9 is by default not connected to the RA6M3 MCU even though it is included on the board. Check section [5.1 SDRAM Selection](#) to see how the SDRAM can be selected.

3.2.3 EEPROM

An EEPROM is also available on the **M13-RA6M3-EK** board. This memory device is controlled by the RA6M3 I²C Interface on channel 0 (IIC0) which is the board's main I²C bus. [Table 11](#) shows the EEPROM Memory Overview. See section [3.11 I²C Interface](#) to have a full illustration on what I²C devices are available on the board.

Table 11. EEPROM Overview

Device Type	MFR ¹ / MPN ²	I ² C Address	Capacity	Package
EEPROM	On Semiconductor / CAT24AA16TDI-GT3	W: 1010 0000 (0xA0) R: 1010 0001 (0xA1)	2048x8 bits (16Kbits)	TSOT-23-5

Table 12. IIC0 Pin assignment

U1 Pin	RA6M3 Pin Functions	Board Assignment	Signal Name	Default Function	Remarks
52	P204 / SCL0_B	Main I ² C bus	SCL0	IIC0	
44	P407 / SDA0_B	Multiplexed	SDA0	IIC0	

3.3 4.3-INCH TFT LCD MODULE

The 4.3-Inch TFT LCD module included in this kit is connected and controlled by the Graphics LCD Controller which by default will output the video image in RGB565 format even though the LCD module is mapped on the complete RGB888 bus. This module comes with a Capacitive touchscreen as shown in [Table 13](#) which is accessible by the SCI6 bus. As for [Table 15](#), it shows the pin assignment between the RA6M3 and the TFT module.

Table 13. TFT LCD Module Overview

Device Type	MFR ¹ / MPN ²	Diagonal Size	Display Format	Package
TFT LCD Module	EastRising /ER-TFT043-3	4.3-Inch	480x272px	N/A

Table 14. Capacitive Touchscreen

Device Type	MFR ¹ / MPN ²	Diagonal Size	I ² C Address	Package
Capacitive Touchscreen	EastRising / ER-TPC043-2	4.3-Inch	W: 0111 0000 (0x70) R: 0111 0001 (0x71)	N/A

Table 15. LCD Assignment Pins

U1 Pin	RA6M3 Pin Functions	Board Assignment	Signal Name	Default Function	ER-TFT043-7 signal
137	P804 / LCD_DATA00_B	LCD	LCD_DATA00_B	LCD	R0
136	P803 / LCD_DATA01_B	LCD	LCD_DATA01_B	LCD	R1
135	P802 / LCD_DATA02_B	LCD	LCD_DATA02_B	LCD	R2
116	P606 / LCD_DATA03_B	LCD	LCD_DATA03_B	LCD	R3
115	P607 / LCD_DATA04_B	LCD	LCD_DATA04_B	LCD	R4
114	PA00 / LCD_DATA05_B	LCD	LCD_DATA05_B	LCD	R5
113	PA01 / LCD_DATA06_B	LCD	LCD_DATA06_B	LCD	R6
109	PA10 / LCD_DATA07_B	LCD	LCD_DATA07_B	LCD	R7
108	PA09 / LCD_DATA08_B	LCD	LCD_DATA08_B	LCD	G0
107	PA08 / LCD_DATA09_B	LCD	LCD_DATA09_B	LCD	G1
106	P615 / LCD_DATA10_B	LCD	LCD_DATA10_B	LCD	G2
73	P905 / LCD_DATA11_B	LCD	LCD_DATA11_B	LCD	G3
72	P906 / LCD_DATA12_B	LCD	LCD_DATA12_B	LCD	G4
71	P907 / LCD_DATA13_B	LCD	LCD_DATA13_B	LCD	G5
70	P908 / LCD_DATA14_B	LCD	LCD_DATA14_B	LCD	G6
59	P901 / LCD_DATA15_B	LCD	LCD_DATA15_B	LCD	G7
174	P513 / LCD_DATA16_B	LCD	LCD_DATA16_B	LCD	B0
173	P805 / LCD_DATA17_B	LCD	LCD_DATA17_B	LCD	B1
66	P208 / LCD_DATA18_B	LCD	LCD_DATA18_B	LCD	B2
65	P209 / LCD_DATA19_B	LCD	LCD_DATA19_B	LCD	B3
64	P210 / LCD_DATA20_B	LCD	LCD_DATA20_B	LCD	B4
63	P211 / LCD_DATA21_B	LCD	LCD_DATA21_B	LCD	B5
62	P214 / LCD_DATA22_B	LCD	LCD_DATA22_B	LCD	B6
49	P207 / LCD_DATA23_B	LCD	LCD_DATA23_B	LCD	B7
57	P315 / LCD_DISP	LCD	LCD_DISP ³	I/O port	DISP
56	P314 / LCD_TCON1_B	LCD	LCD_TCON1_B	LCD	HSYNC
55	P313 / LCD_TCON2_B	LCD	LCD_TCON2_B	LCD	VSYNC
54	P202 / LCD_TCON3_B	LCD	LCD_TCON3_B	LCD	DE ⁴
58	P900 / LCD_CLK_B	LCD	LCD_CLK_B	LCD	PLCK

Note 1: Manufacturer name

Note 2: Manufacturer Part Number

Note 3: Connected to the LCD Display signal and configured as a general GPIO in output mode with an On/Off behaviour.

Note 4: Data Enable

The LCD signal inputs are assigned in RGB888 format and connected onto the RA6M3 in BGR, little Indian arrangement.

3.4 USB INTERFACE

The two USB modules, USBFS (Full-Speed) and USBHS, (High-Speed) from the RA6M3 are being used on this board. Either of them can be used as a USB HOST or a USB DEVICE port, thus Micro A/B connectors type are being used for each module.

When the USBFS or the USBHS are being used in Host mode, respectively, JP9 or JP1 must be connected. On the other hand, leave each of them opened if you want each module to function as a USB device mode. [Figure 9](#) illustrates the USB Interface general diagram while [Table 17](#) gives you the RA6M3 pin assignments. As we lacked the available pins, OTG functions are not mapped nor used.

Figure 9. USB Diagram

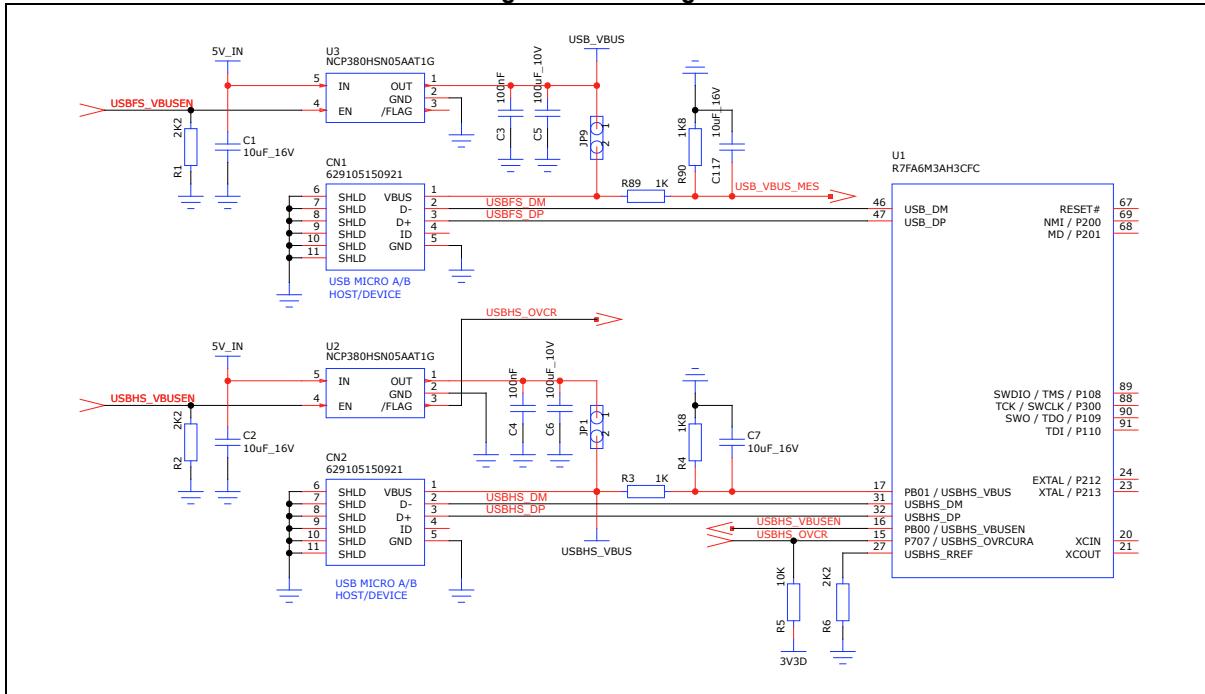


Table 16. USB Overview

Device Type	MFR ¹ / MPN ²	Package	Note
USB Micro A/B	Würth Electronics / 629105150921	SMD ³ , Right Angle	CN1
USB Micro A/B	Würth Electronics / 629105150921	SMD ³ , Right Angle	CN2

Table 17. USB Pin Assignment

U1 Pin	RA6M3 Pin Functions	Board Assignment	Signal Name	Default Function	Note
44	P407 / USB_VBUS	Multiplexed	USBFS_VBUS_MES	IIC0	
46	USB_DM	USB	USBFS_DM	USBFS	
47	USB_DP	USB	USBFS_DP	USBFS	
151	P014 / AN005 / AN105	USB	USBFS_VBUSEN ⁴	I/O port ⁴	
17	PB01 / USBHS_VBUS	USB	USBHS_VBUS	USBHS	
31	USBHS_DM	USB	USBHS_DM	USBHS	
32	USBHS_DP	USB	USBHS_DP	USBHS	
16	PB00 / USBHS_VBUSEN	USB	USBHS_VBUSEN	USBHS	
15	P707 / USBHS_OVRCURA	USB	USBHS_OVRCURA	USBHS	
27	USBHS_RREF	USB	USBHS_RREF	USBHS	

Note 1: Manufacturer name

Note 2: Manufacturer Part Number

Note 3: Surface Mount Device

Note 4: As the VBUSEN pin for the USBFS module is not available due to being used by other peripherals, P014 is configured as a GPIO to ensure the said function.

3.5 LAN INTERFACE

The **M13-RA6M3-EK** embarks an Ethernet PHY (U7) which communicate through the RA6M3 on-chip ethernet controller ETHERC by using the RMII Interface. The details of this device can be seen in [Table 18](#). As for the RMII pin assignment they are displayed in [Table 19](#).

Table 18. Ethernet PHY Overview

Device Type	MFR ¹ / MPN ²	Operational Voltage	Bit Rate	Package
Ethernet PHY	Microchip / KSZ8081RNA	3.3V	10 Mbps / 100 Mbps	N/A
RJ45 Connector	Wurth Elektronik / 7499011121A	N/A	N/A	Through-Hole

Note 1: Manufacturer name

Note 2: Manufacturer Part Number

Table 19. Ethernet Assignment Pins

U1 Pin	RA6M3 Pin Functions	Board Assignment	Signal Name	Default Function	Remarks
14	P706 / IRQ7	Multiplexed	ET0_IRQ7	SD1CD	
36	P415 / RMII0_TXDEN_A	Ethernet	RMII0_TXDEN_A	ETHERC (RMII)	
37	P414 / RMII0_TXD1_A	Ethernet	RMII0_TXD1_A	ETHERC (RMII)	
38	P413 / RMII0_RXD0_A	Ethernet	RMII0_RXD0_A	ETHERC (RMII)	
42	P409 / RMII0_RX_ER_A	Ethernet	RMII0_RX_ER_A	ETHERC (RMII)	
43	P408 / RMII0_CRS_DV_A	Ethernet	RMII0_CRS_DV_A	ETHERC (RMII)	
39	P412 / REF50_CK0_A	Ethernet	REF50_CK0_A	ETHERC (RMII)	
41	P410 / RMII0_RXD1_A	Ethernet	RMII0_RXD1_A	ETHERC (RMII)	
40	P411 / RMII0_RXD0_A	Ethernet	RMII0_RXD0_A	ETHERC (RMII)	
2	P401 / ET0_MDC	Ethernet	ET0_MDC	ETHERC (RMII)	
3	P402 / ET0_MDIO	Ethernet	ET0_MDIO	ETHERC (RMII)	
172	P806	Ethernet	ET0_LED2	I/O port	

P806 is configurated as a standard output to drive the second led available on the RJ45 connector CN6 through its pin LED2-. And as described in table 18, P706 is by default not connected to the Ethernet PHY IRQ signal (Pin U7.18) but rather to the SD Card “Card Detection” pin (CN10.9). Follow [Table 20](#) if you need interrupt capabilities on your Ethernet Interface.

Table 20. P706 Multiplexing

RA6M3 Pin	RA6M3 Pin Description	Selected Function	SH41	SH42
14	P706 / SD1CD / IRQ7	ET0_IRQ7	Not Fitted	Fitted
		SD1CD (Default)	Fitted	Not Fitted

3.6 SD/MMC HOST INTERFACE (4-BITS)

The **M13-RA6M3-EK** board embarks a microSD card connector which is connected to the RA6M3's SD/MMC Host Interface on channel 1 as shown in [Figure 10](#) and [Table 21](#) and uses a 4-bit wide interface. The SD card detection and write protection signals are not mapped and not used.

Figure 10. SD/MMC Host Interface Diagram

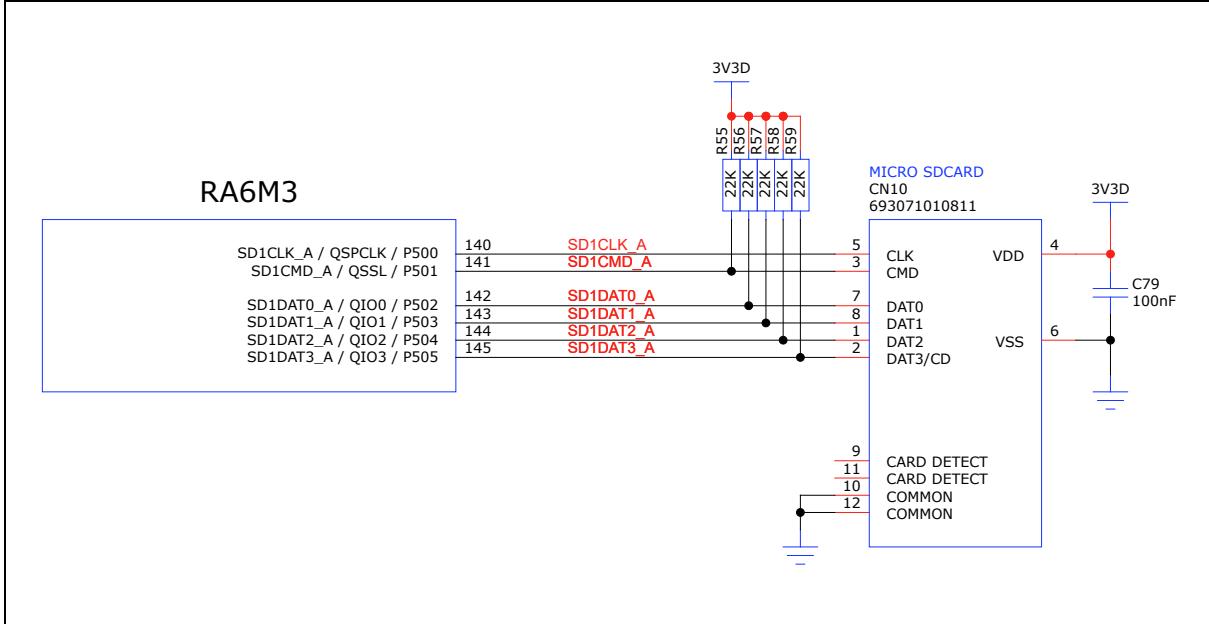


Table 21. SD/MMC Interface Pin Assignment

U1 Pin	RA6M3 Pin Functions	Board Assignment	Signal Name	Default Function	Remarks
140	P500 / SD1CLK_A / QSPCLK	JP3	SD1CLK_A	QSPI	Multiplexed
141	P501 / SD1CMD_A / QSSL	JP4	SD1CMD_A	QSPI	Multiplexed
142	P502 / SD1DAT0_A / QIO0	JP5	SD1DAT0_A	QSPI	Multiplexed
143	P503 / SD1DAT1_A / QIO1	JP6	SD1DAT1_A	QSPI	Multiplexed
144	P504 / SD1DAT2_A / QIO2	JP7	SD1DAT2_A	QSPI	Multiplexed
145	P505 / SD1DAT3_A / QIO3	JP8	SD1DAT3_A	QSPI	Multiplexed

The microSD card is connected to the RA6M3 through the JP3-JP8 jumpers. See [Section 5.2 SD CARD](#) for detailed information on multiplexing the P500-P505 signals.

3.7 AUDIO INTERFACE

The **M13-RA6M3-EK** is equipped with a Maxim Audio CODEC (U13) for audio features. Its configurations and controls are done through the I²C interface using channel 0. While the exchange of audio data is done using the Serial Sound Interface (SSIE) channel 0.

The output uses a single 4-pole 3.5mm audio jack connector for connecting a headset in single-ended mode. See section [4.9 CN11: 4-Pole Audio Jack](#) for a detailed description on the headset configuration.

As the Audio CODEC is configured and used in Master Mode, its operating clock is directly provided from an external 13MHz oscillator and not from the RA6M3. See [Table 22](#) for the Audio CODEC details, [Table 23](#) for its pin assignment and [Figure 11](#) for a full illustration of the Audio Block Diagram.

Table 22. Audio CODEC Overview

Device Type	MFR ¹ / MPN ²	Operational Voltage	I ² C Address	Package
Audio CODEC	Maxim / MAX9867ETJ	1.8V	W: 0011 0000 (0x30) R: 0011 0001 (0x31)	QFN32

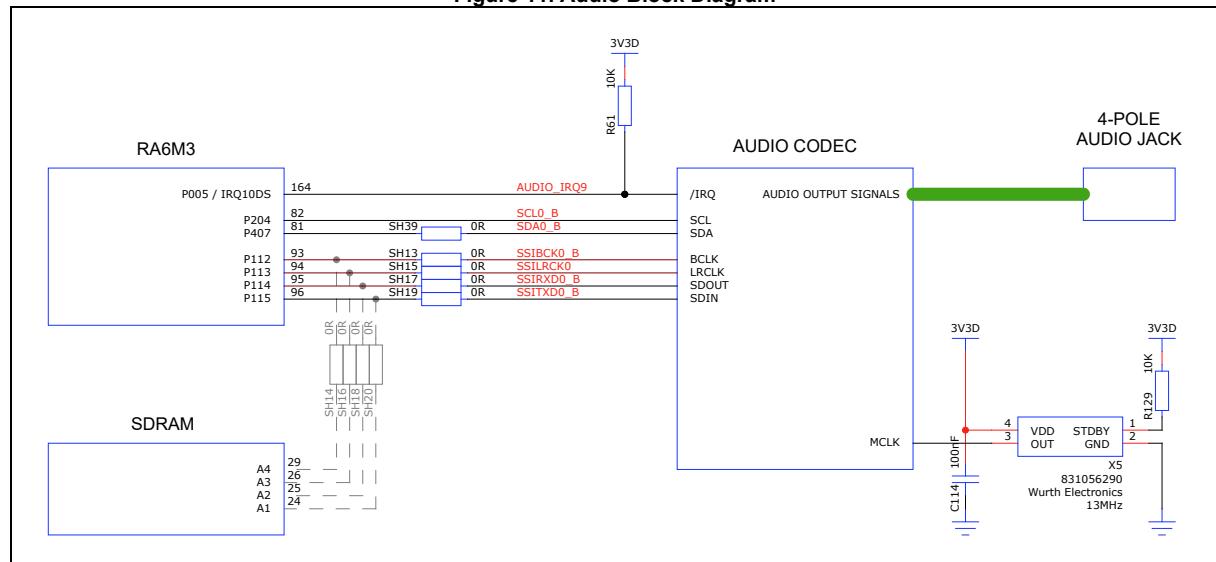
Note 1: Manufacturer name

Note 2: Manufacturer Part Number

Table 23. Audio Pin Assignment

U1 Pin	RA6M3 Pin Functions	Board Assignment	Signal Name	Default Function	Remarks
165	P004 / IRQ9DS	IRQ9DS	AUDIO_IRQ9	IRQ	
95	P114 / SSIRXD0_B / A02	Multiplexed	SSIRXD0_B	SSIE0	
96	P115 / SSITXD0_B / A01	Multiplexed	SSITXD0_B	SSIE0	
94	P113 / SSILRCK0 / A03	Multiplexed	SSILRCK0	SSIE0	
93	P112 / SSIBCK0_B / A04	Multiplexed	SSIBCK0_B	SSIE0	
52	P204 / SCL0_B	Main I ² C bus	SCL0	IIC0	
44	P407 / SDA0_B	Multiplexed	SDA0	IIC0	
N/A	N/A	N/A	AUDIO_MCLK	N/A	X5 – 13MHz

Figure 11. Audio Block Diagram



See section [5.1.2ADDR](#) for a full description of the multiplexed GPIOs of the SSIE bus.

3.8 3-AXIS ACCELEROMETER

The **M13-RA6M3-EK** board is equipped with a 3-Axis Accelerometer from Würth Electronics. This device is controlled by the RA6M3 I²C Interface on channel 0 (IIC0) as shown in [Table 25](#). [Table 24](#) shows the device overview.

Table 24. Accelerometer Overview

Device Type	MFR ¹ / MPN ²	I ² C Address	Scale	Package
Accelerometer	Würth Electronics / 2533020201601	W: 0011 0000 (0x32) R: 0011 0001 (0x33)	±2g, ±4g, ±8g, ±16g	LGA12 2.0x2.0x 0.7 mm

Table 25. IIC0 Pin assignment

U1 Pin	RA6M3 Pin Functions	Board Assignment	Signal Name	Default Function	Remarks
52	P204 / SCL0_B	Main I ² C bus	SCL0	IIC0	
44	P407 / SDA0_B	Multiplexed	SDA0	IIC0	

3.9 J-LINK OB

The **M13-RA6M3-EK** board embarks a J-Link OB from Segger, which is the board's default debugging and programming probe. The J-Link OB supports JTAG, SWD (+SWO) and one VCOM interface. Through its USB connector (CN5) the J-Link OB is also the board main 5VDC power supply.

[Figure 12](#) illustrate the overall configuration of the debug interface of the board. And [Table 26](#) shows you the detailed pin assignment between the RA6M3 and the JTAG/SWD signals bus.

Figure 12. Debug Interface Diagram

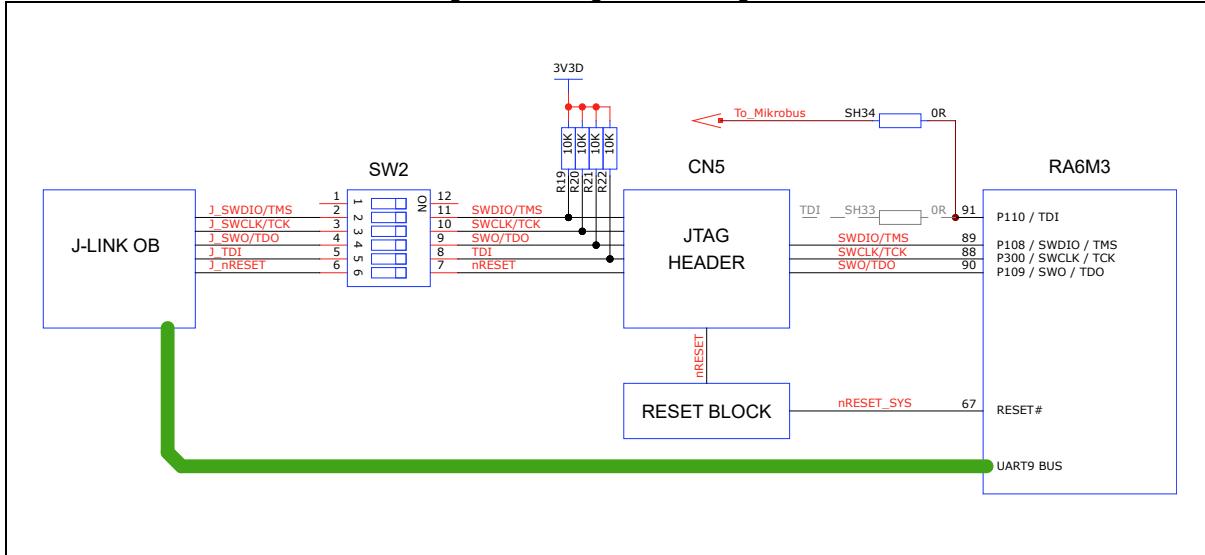


Table 26. SWD/JTAG Pin Assignment

U1 Pin	RA6M3 Pin Functions	Board Assignment	Signal Name	Default Function	Remarks
89	P108 / SWDIO / TMS	Debug	SWDIO/TMS	SWD	
88	P300 / SWCLK / TCK	Debug	SWCLK/TCK	SWD	
90	P109 / SWO / TDO	Debug	SWO/TDO	SWD	
91	P110 / TDI	Multiplexed	P110	MIKROBUS	
51	P205 / TXD4	VCOM	TXD4	VCOM	
50	P206 / TXD4	VCOM	RXD4	VCOM	

The reset signal from the J-Link OB is not detailed in this section. You will find a complete description of this signal in section [3.1.2.System Reset pin](#).

As stated in [Table 26](#), the J-Link OB is configurated by default in SWD protocol. To switch to JTAG, solder SH33 and remove SH34 as described in section [5.3 TDI / CTS2 / IRQ11](#).

While assuming you already have the J-Link OB probe drivers installed on your PC, [Table 27](#) shows you the configurations and status for using the on-board debugger or if needed other third-party ones.

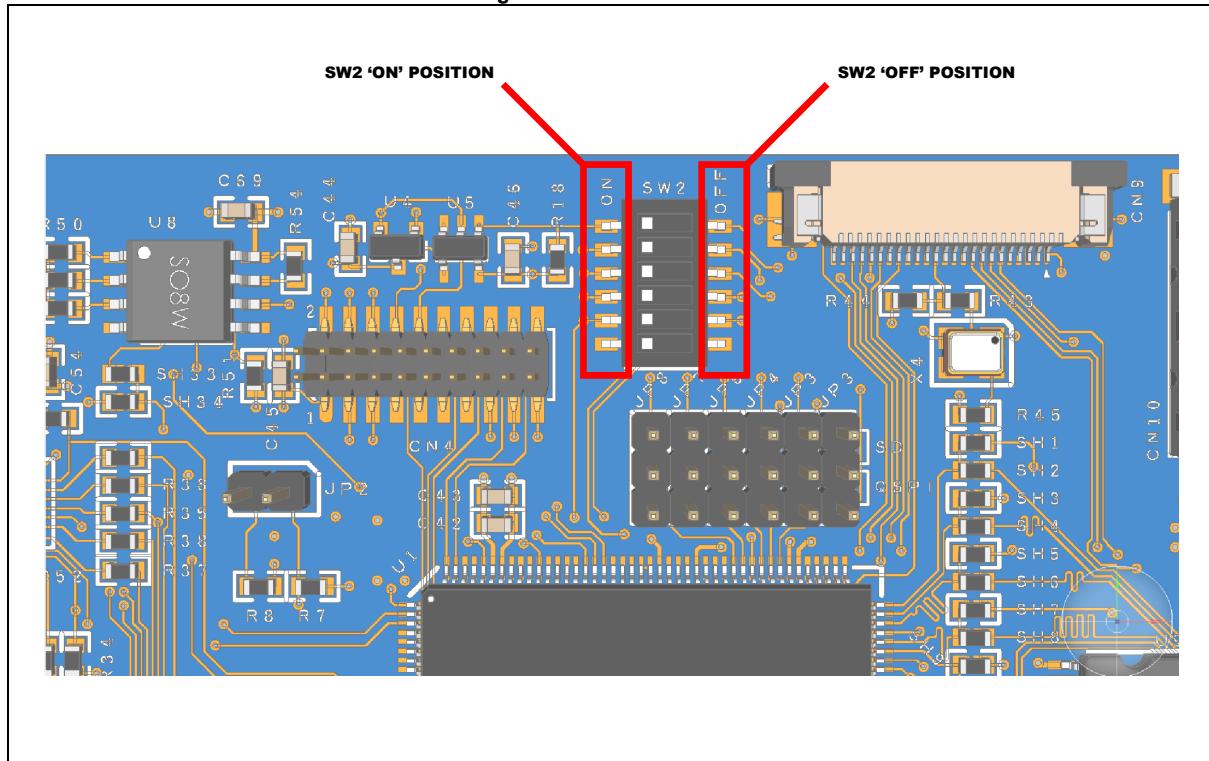
Table 27. Debug Configuration

Probe used for debug	SW2.2 to SW2.6	D4 (Status Led)	Remarks
J-Link OB (Default)	On	Turned on	SW2.1 is not used
External JTAG Probe	Off	Blinking ¹	

Note 1: D4 will keep blinking until the J-Link OB is connected to a computer USB port through CN5

In order to use the J-Link OB, make sure to slide all the SW2 switches on the “On” position. See [Figure 13](#), which represents the PCB Top side, to have a better visualization of the “On/Off” positioning of SW2.

Figure 13. SW2 Illustration



3.10 VGA CAMERA MODULE

The **M13-RA6M3-EK** board is also capable to drive VGA camera modules with its Parallel Data Capture Unit (PDC). Through the connector CN8, we provide an 8-bit interface which is compatible with many modules actually on the market. [Table 29](#) shows the RA6M3 pin assignments. For details on the connector, see section [4.7 CN9: 8 Bit VGA Camera](#) module.

Table 28. VGA Camera Module Overview

Device Type	MFR ¹ / MPN ²	I ² C Address	Package	Note
VGA Camera	TD Next / TD7740	W: 0010 0000 (0x42) R: 0010 0001 (0x43)	N/A	
Connector	Würth Electronics / 68712414022	N/A	SMD, 0.50mm Right angle 24 pin - Top contact	CN8

Note 1: Manufacturer name

Note 2: Manufacturer Part Number

Table 29. 8bit VGA Interface Pin Assignment

U1 Pin	RA6M3 Pin Functions	Board Assignment	Signal Name	Default Function	Remarks
44	P407 / SDA0_B / USB_VBUS	Multiplexed	SDA0_B	IIC0	
52	P204 / SCL0_B	Main I ² C bus	SCL0_B	IIC0	
147	P507 / AN119	Camera	CAM_RST	GPIO	
148	P508 / AN020	Camera	CAM_PWR_DN	GPIO	
174	P512 / VSYNC	Camera	VSYNC	PDC	
12	P703 / HSYNC	Camera	HSYNC	PDC	
176	P511 / PCKO	Multiplexed	XLCK	PDC / PCKO	
13	P705 / PIXCLK	Camera	PIXCLK	PDC	
4	P403 / PIXD7	Camera	PIXD7	PDC	
5	P404 / PIXD6	Camera	PIXD6	PDC	
6	P405 / PIXD5	Camera	PIXD5	PDC	
7	P406 / PIXD4	Camera	PIXD4	PDC	
8	P700 / PIXD3	Camera	PIXD3	PDC	
9	P701 / PIXD2	Camera	PIXD2	PDC	
10	P702 / PIXD1	Camera	PIXD1	PDC	
11	P703 / PIXD0	Camera	PIXD0	PDC	

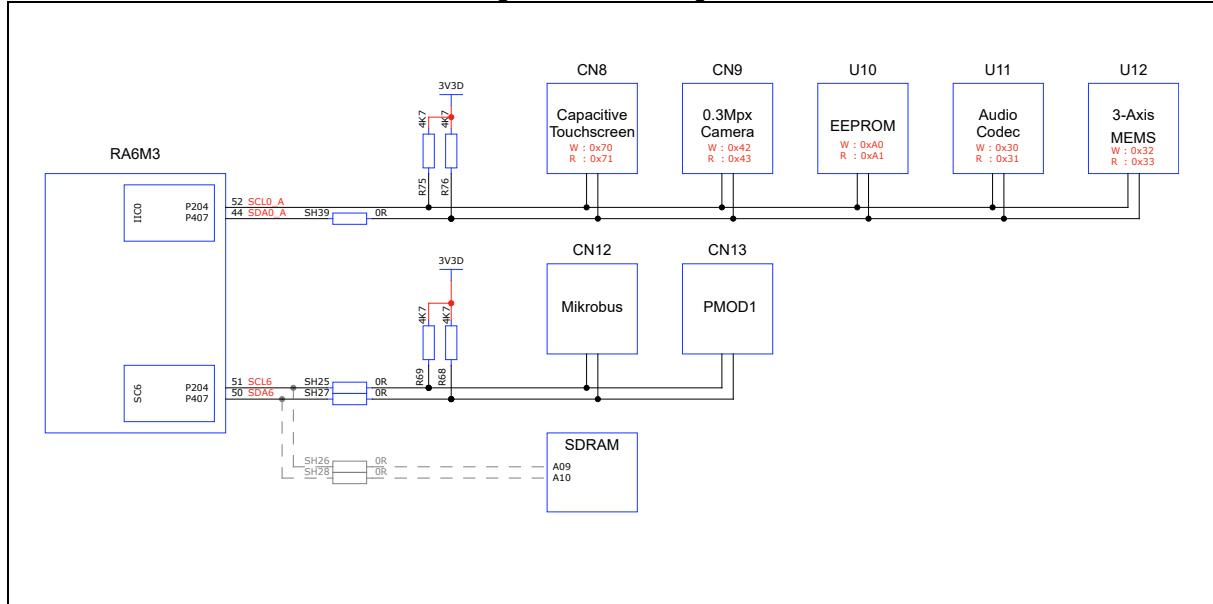
3.11 I²C INTERFACE

The **M13-RA6M3-EK** board uses two I²C channels which are divided between the I²C Bus Interface module (IIC) and the Serial Communication Interface (SCI). **Table 30** shows you how each of these channels are mapped on the board.

Table 30. I²C pin assignment

U1 Pin	RA6M3 Pin Functions	Board Assignment	Signal Name	Default Function	Remarks
52	P204 / SCL0_B	Main I ² C Bus	SCL0_B	IIC0	
44	P407 / USB_VBUS	Main I ² C Bus	SDA0_B	IIC0	Multiplexed
82	P304 / SCL9 / A09	Multiplexed	SCL6	SCI6	
81	P305 / SDA9 / A10	Multiplexed	SDA6	SCI6	

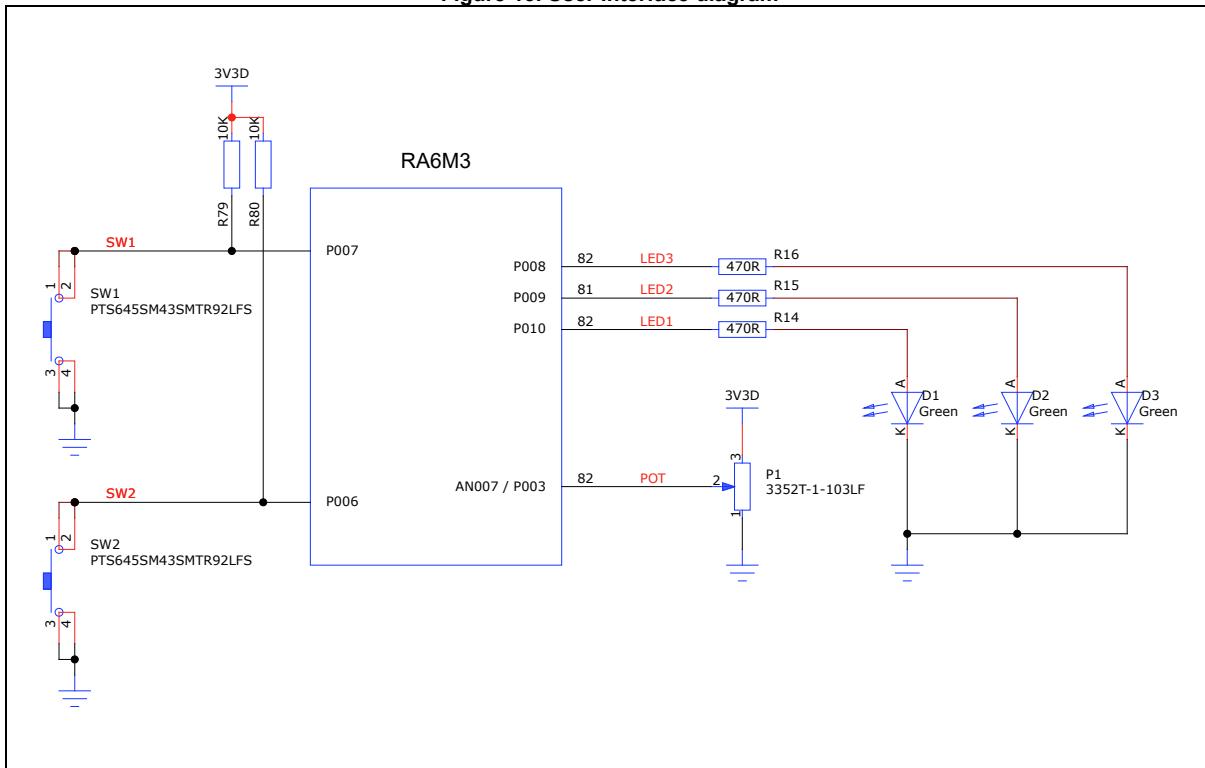
Figure 14. I²C bus diagram



As illustrated in [Figure 14](#) the IIC channel 0 is the board's main I²C bus and is by default selected by the resistor shunt SH39. The mikroBUS™ and the PMOD1 share the same I²C bus and is by default selected with the SH25 and SH27 resistor shunts.

3.12 USER INTERFACE: SWITCH, LED, POTENTIOMETER

Figure 15. User Interface diagram



The **M13-RA6M3-EK** board contains 2 User Switches and 3 User Leds (Green coloured) as described in [Table 32](#) and is also equipped with a 10K mono-turn Potentiometer.

Table 31. User Interface Overview

Device Type	MFR ¹ / MPN ²	REFERENCE	Package	Remarks
User Switch	C&K / KSC701JLFS	SW1 / SW2	SMD, Top Switch	
User Leds	Wurth Electronics / 150060VS55040	D1/D2/D3	SMD D0603	

Note 1: Manufacturer name

Note 2: Manufacturer Part Number

Table 32. User Interface Pin Assignment

U1 Pin	RA6M3 Pin Functions	Board Assignment	Signal Name	Default Function	Remarks
162	P007	USER_SWITCH	SW1	Input	
163	P006	USER_SWITCH	SW2	Input	
159	P010	USER_LED	LED1	Output	
160	P009	USER_LED	LED2	Output	
161	P008	USER_LED	LED3	Output	
166	P003 / AN007	POTENTIOMETER	POT	ADC12	

4 CONNECTOR OVERVIEW

4.1 CN1: USB-MICRO A/B

Figure 16. CN1: USB-Micro A/B Front view



Table 33. CN1 Pin Description

CN1 Pin	Pin Description	Signal Name	RA6M3 Pin	Note
1	VBUS	CN1_VBUS	-	
2	D-	USBFS_DM	46	
3	D+	USBFS_DP	47	
4	ID	N/A	-	
5	GND	GND	-	

4.2 CN2: USB-MICRO A/B

Figure 17. CN2: USB- Micro A/B Front view



Table 34. CN2 Pin Description

CN2 Pin	Pin Description	Signal Name	RA6M3 Pin	Note
1	VBUS	CN2_VBUS	-	
2	D-	USBHS_DM	31	
3	D+	USBHS_DP	32	
4	ID	N/A	-	
5	GND	GND	-	

4.3 CN4: 19-PIN JTAG HEADER

Figure 18. CN4: 19-pin JTAG Header

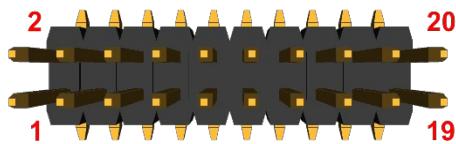


Table 35. CN4 Pin Assignment

CN4 Pin	Pin Description	Signal Name	RA6M3 Pin	Note
1	VTREF	3V3D	-	
2	SWDIO/TMS	SWDIO / TMS	89	
3	GND	GND	-	
4	SWCLK/TCK	SWCLK / TCK	88	
5	GND	GND	-	
6	SWO/TDO	SWO / TDO	90	
7	Not used	Not used	-	
8	TDI	TDI	91	Multiplexed
9	NC	NC	-	
10	nRESET	nRESET	-	
11	VCC	Not used	-	
12	P214 / TCLK	TCLK	-	Multiplexed
13	VCC	Not used	-	
14	P211 / TDATA0	TDATA0	-	Multiplexed
15	GND	GND	-	
16	P210 / TDATA1	TDATA1	-	Multiplexed
17	GND	GND	-	
18	P209 / TDATA2	TDATA2	-	Multiplexed
19	GND	GND	-	
20	P208 / TDATA3	TDATA3	-	Multiplexed

4.4 CN6: RJ45

Figure 19. CN6. RJ45 Bottom View

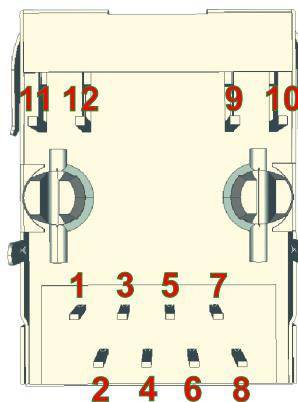


Table 36. CN6 Pin Assignment

CN6 Pin	Pin Description	Signal Name	U7 Pin	Note
1	TD+	TXP	6	
2	TCT	-	-	
3	TD-	TXM	5	
4	RD+	RXP	4	
5	RCT	-	-	
6	RD-	RXM	3	
7	NC	-	-	
8	COM	GND	-	
9	LED1+	3V3D	-	
10	LED1-	-	23	
11	LED2+	3V3D	-	
12	LED2-	ET0 LED2	-	P806

4.5 CN7: LCD CONNECTOR

Figure 20. CN7. Front View

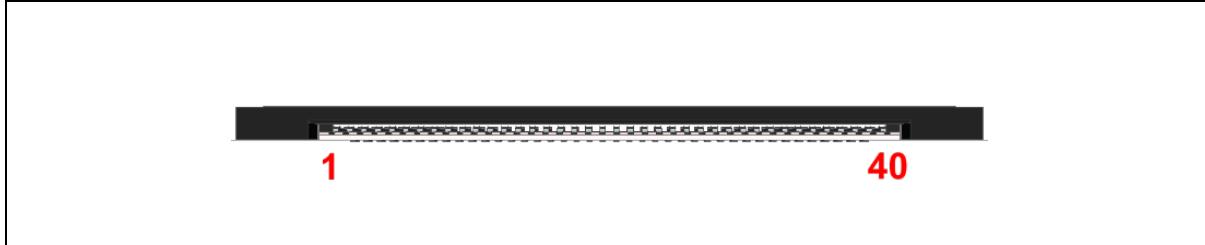


Table 37. CN7 Pin Assignment

CN7 Pin	CN7 Pin Description	Signal Name	RA6M3 Pin	Note
1	VLED-	VLED-	-	From U13
2	VLED+	VLED+	-	From U13
3	GND	GND	-	
4	VDD	3V3D	-	
5	R0	LCD_DATA00_B	137	
6	R1	LCD_DATA01_B	136	
7	R2	LCD_DATA02_B	135	
8	R3	LCD_DATA03_B	116	
9	R4	LCD_DATA04_B	115	
10	R5	LCD_DATA05_B	114	
11	R6	LCD_DATA06_B	113	
12	R7	LCD_DATA07_B	109	
13	G0	LCD_DATA08_B	108	
14	G1	LCD_DATA09_B	107	
15	G2	LCD_DATA10_B	106	
16	G3	LCD_DATA11_B	73	
17	G4	LCD_DATA12_B	72	
18	G5	LCD_DATA13_B	71	
19	G6	LCD_DATA14_B	70	
20	G7	LCD_DATA15_B	59	
21	B0	LCD_DATA16_B	174	
22	B1	LCD_DATA17_B	173	
23	B2	LCD_DATA18_B	66	
24	B3	LCD_DATA19_B	65	
25	B4	LCD_DATA20_B	64	
26	B5	LCD_DATA21_B	63	
27	B6	LCD_DATA22_B	62	
28	B7	LCD_DATA23_B	49	
29	GND	GND	-	
30	PLCK	LCD_CLK_B	58	
31	DISP	LCD_DISP	57	I/O Port
32	HSYNC	LCD_TCON1_B	56	
33	VSYNC	LCD_TCON2_B	55	
34	DE	LCD_TCON3_B	54	
35	NC	None	-	
36	GND	GND	-	
37	XR	None	-	
38	YD	None	-	
39	XL	None	-	
40	YU	None	-	

4.6 CN8: LCD CAPACITIVE TOUCH

Figure 21. CN8 Front View



Table 38. CN8 Pin Assignment

CN8 Pin	Pin Description	Signal Name	RA6M3 Pin	Note
1	SCL	SCL0_B	52	
2	SDA	SDA0_B	44	
3	VDD	3V3D	-	
4	RST	nRESET_SYS	67	
5	INT	TOUCH_IRQ06	169	
6	GND	GND	-	

4.7 CN9: 8 BIT VGA CAMERA MODULE

Figure 22. CN9 Front View



Table 39. CN9 Pin Assignment

CN9 Pin	Pin Description	Signal Name	RA6M3 Pin	Note
1	SFIN	None	-	Pulled-down
2	AGND	GND	-	
3	SDA	SDA0_B	52	SIOD
4	AVDD	GND	-	
5	SCL	SCL0_B	44	SIOC
6	/RST	CAM_RST	147	
7	VSYNC	VSYNC	175	
8	PWDN	CAM_PWR_DN	148	
9	HSYNC	Hsync	12	HREF
10	VCORE	None	-	100nF to GND
11	DVDD	3V3D	-	
12	Y9	PIXD7	4	
13	XCLK	XLCK	176	multiplexed
14	Y8	PIXD6	5	
15	DGND	GND	-	
16	Y7	PIXD5	6	
17	PCLK	PIXCLK	13	
18	Y6	PIXD4	7	
19	Y2	PIXD0	11	
20	Y5	PIXD3	8	
21	Y3	PIXD1	10	
22	Y4	PIXD2	9	
23	Y1	None	-	Not used
24	Y0	None	-	Not used

4.8 CN10: MICRO SD CARD

Figure 23. CN10: MicroSD Card Bottom View

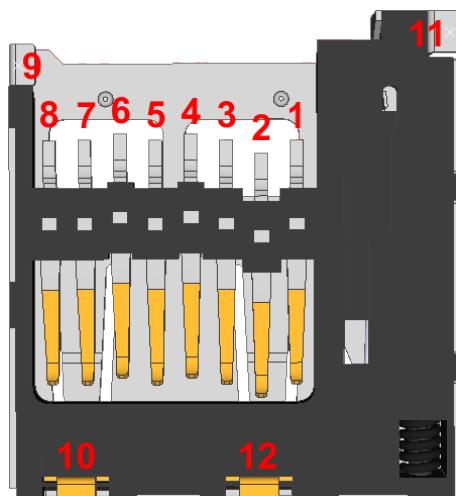


Table 40. CN10: Micro SD Card Pin Assignment

CN10 Pin	Pin Description	Signal Name	RA6M3 Pin	Note
1	DAT2	SD1DAT2_A	144	Multiplexed
2	DAT3/CD	SD1DAT3_A	145	Multiplexed
3	CMD	SD1CMD_A	141	Multiplexed
4	VDD	3V3D	-	
5	CLK	SD1CLK_A	140	Multiplexed
6	VSS	GND	-	
7	DAT0	SD1DAT0_A	142	Multiplexed
8	DAT1	SD1DAT1_A	143	Multiplexed
9 & 11	CARD DETECT	None	-	
10 & 12	COMMON	GND	-	

4.9 CN11: 4-POLE AUDIO JACK

Figure 24. CN11 Mating Plug and Bottom View

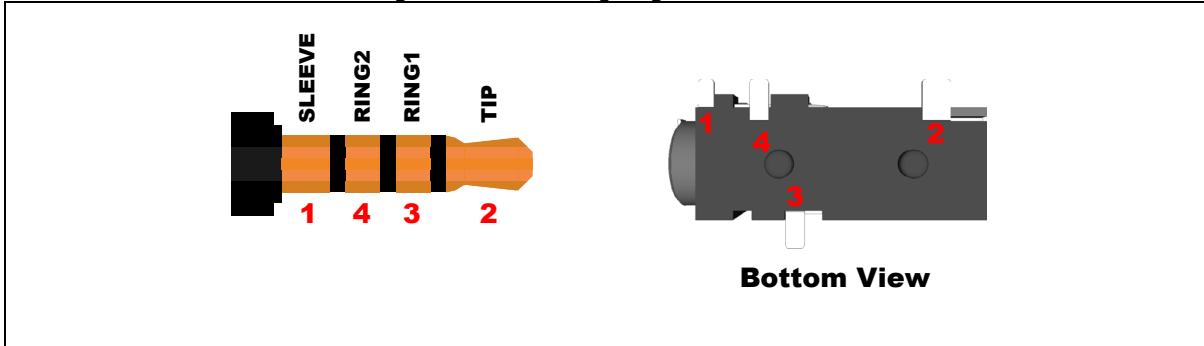


Table 41. CN11 Pin Assignment

CN11 Pin	Pin Description	Signal Name	U11 Pin	Note
1	SLEEVE	MIC	12	
2	TIP	LEFT	22	Single ended
3	RING1	RIGHT	19	Single ended
4	RING2	GND	GND	

4.10 CN12: EXPANSION CONNECTOR - MIKROBUS

Figure 25. CN12 mikroBUS™ Top view

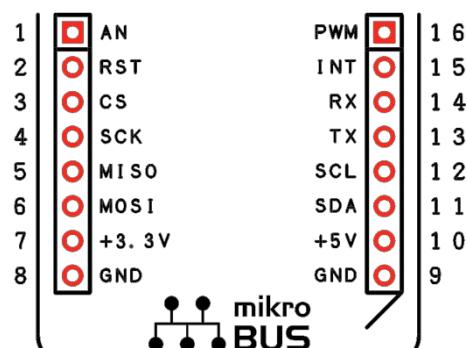


Table 42. CN12 Pin Assignment

CN12 Pin	Pin Description	Signal Name	RA6M3 Pin	Default Function	RA6M3 Pin Description
1	AN	MIKROBUS_AN	168	ADC12	P001 / AN001
2	RST	MIKROBUS_RST	1	I/O Port	P400
3	CS	CTS2_RTS2	53	SCI2 / RTS2	P203
4	SCK	RSPCKA_A	130	SPI0	P102
5	MISO	MISOA_A	132	SPI0	P100
6	MOSI	MOSIA_A	131	SPI0	P101
7	+3.3V	3V3D	-	-	-
8	GND	GND	-	-	-
9	GND	GND	-	-	-
10	+5V	5V_IN	-	-	-
11	SDA	SDA6	82	SCI6	P305 Multiplexed
12	SCL	SCL6	81	SCI6	P304 Multiplexed
13	TX	TXD2	86	SCI2	P302 Multiplexed
14	RX	RXD2	87	SCI2	P301 Multiplexed
15	INT	MIKROBUS_INT	91	SCI2 / CTS2	P110 Multiplexed
16	PWM	MIKROBUS_GTI0C6B	122	GPT	P600

Table 43. mikroBUS™ Overview

Device Type	MFR ¹ / MPN ²	Package	Note
MikroBUSTM Connector	Wurth Electronics / 61300811821	2.54mm	CN12.1 & CN12.2 ³

Note 1: Manufacturer name

Note 2: Manufacturer Part Number

Note 3: For manufacturing purposes CN12 is separated into 2 references CN12.1 and CN12.2 in the Bill of Materials.

4.11 CN13/CN14: EXPANSION CONNECTORS – PMOD

Figure 26. PMOD Front View

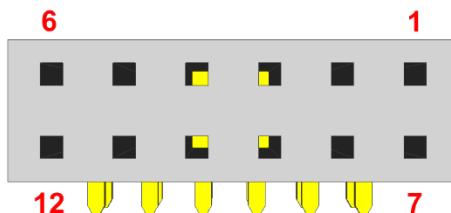


Table 44. PMOD Connector Overview

Device Type	MFR ¹ / MPN ²	Package	Note
PMOD Connector	Wurth Electronics / 613012243121	TH RA 2.54mm	

Table 45. CN13 (PMOD1) Pin Assignment

CN13 Pin	Pin Description	Signal Name	RA6M3 Pin	Default Function	RA6M3 Pin Description
1	CS	SSLA1_A	128	SPI0	P104
2	MOSI	MOSIA_A	131	SPI0	P101
3	MISO	MISOA_A	132	SPI0	P100
4	SCK	RSPCKA_A	130	SPI0	P102
5	GND	GND	-	-	-
6	VCC	3V3D	-	-	-
7	GPIO/INT	PMOD1_IRQ8	167	IRQ8DS	P002
8	GPIO/RST	PMOD1_RST	146	I/O Port	P506
9	GPIO/CS2	SCL6	82	SCI6	P304
10	GPIO/CS3	SDA6	81	SCI6	P305
11	GND	GND	-	-	-
12	VCC	3V3D	-	-	-

The PMOD1 connector is compatible with the **Type 2** (SPI) interface and with the **Type 2A** (Expanded SPI) interface if the I²C SCI6 bus is not used by the mikroBUS™ connector. It can also be used as a **Type 6** (I²C) on pin 7-12. Remove SH37 and SH38 if you encounter any conflict while using both the PMOD1 and the mikroBUS™ interfaces.

Table 46. CN14 (PMOD2) Pin Assignment

CN14 Pin	Pin Description	Signal Name	RA6M3 Pin	Default Function	RA6M3 Pin Description
1	CS	SSLA2_A	127	SPI0	P105
2	MOSI	MOSIA_A	131	SPI0	P101
3	MISO	MISOA_A	132	SPI0	P100
4	SCK	RSPCKA_A	130	SPI0	P102
5	GND	GND	-	-	-
6	VCC	3V3D	-	-	-
7	GPIO/INT	PMOD2 IRQ10	164	IRQ10	P005
8	GPIO/RST	PMOD2_RST	92	GPIO	P111
9	GPIO/CS2	RPMOD_IO9	52	GPIO	P601
10	GPIO/CS3	RPMOD_IO10	44	GPIO	P602
11	GND	GND	-	-	-
12	VCC	3V3D	-	-	-

The PMOD2 connector is compatible with the **Type 2** (SPI) interface and with the **Type 2A** (Expanded SPI) interface.

4.12 CN15: +5VDC POWER JACK

Figure 27. CN15 Power Jack

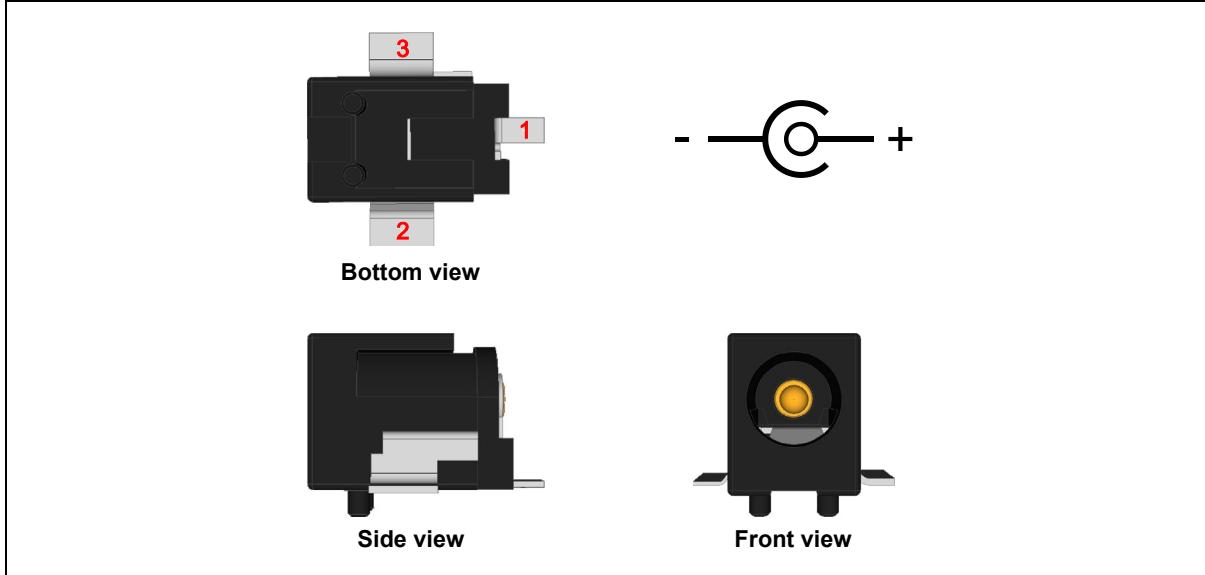


Table 47. CN15 Connector Overview

Device Type	MFR ¹ / MPN ²	Package	Note
PMOD Connector	Wurth Electronics / 694106105102	SMD Right Angle	

Note 1: Manufacturer name

Note 2: Manufacturer Part Number

Table 48. CN15 Pin Assignment

CN15 Pin	Pin Description	Signal Name	Note
1	Center Pin	V_JACK	Strictly +5VDC
2	Outer Ring	GND	
3	Detect	-	Note used

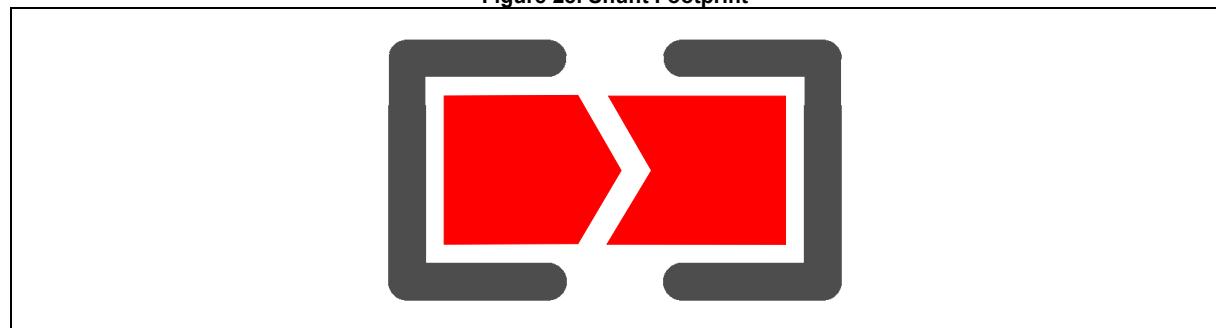
5 MULTIPLEXED FUNCTIONS

In order to propose the largest panel of functions possible to the user, we have multiplexed and mapped a maximum of the RA6M3 pins towards the board's devices and peripherals. Some of these functions can be selected by removing/soldering multiple shunts on the board. By default, the SDRAM, the SD Card, the CTS2 mikroBUSTM and the USBFS VBUS pins are deactivated and not connected to the RA6M3. [Table 49](#) shows you which functions are multiplexed between which peripherals/devices.

Table 49. Multiplexing Function Table

	SDRAM	SD CARD	mikroBUS CTS2		USBFS
Serial Flash		QSPI/SDHI			
JTAG			TDI / CTS2 / IRQ11		
mikroBUS	DATA / SPI0				
PMOD1					
PMOD2					
Main I ² C SDA					SDA0_B / USB_VBUS
SSIE: Audio Codec	ADDR / SSIE0				
mikroBUS: UART	ADDR / SCI2				
mikroBUS: I ² C	ADDR / SCI6				
PMOD1					
PMOD2		A05 / RST DQM0 / IO9 SDCLK / IO10			

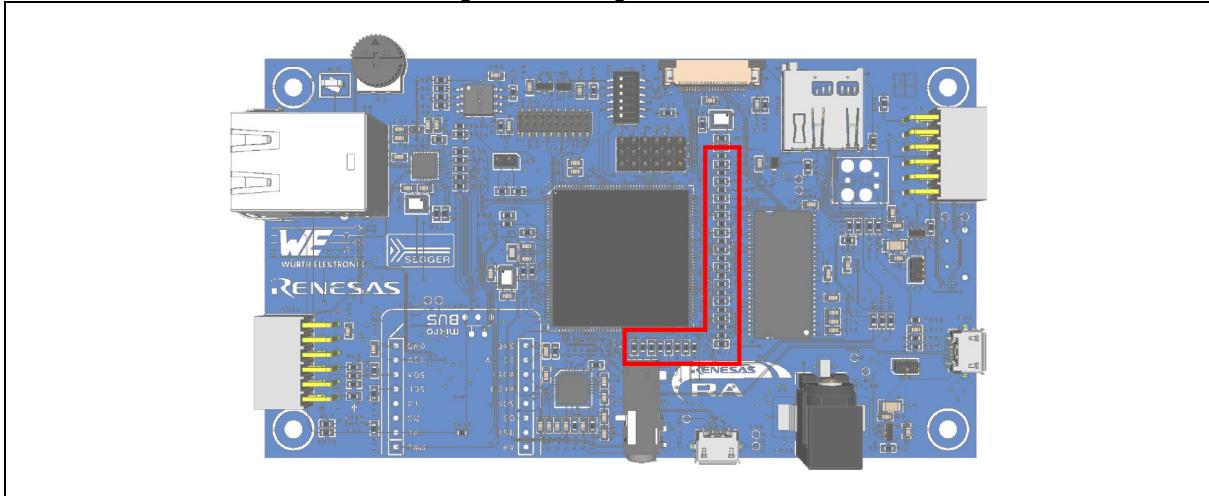
The Sections 5.1 to 5.4 describe you how each function can be selected and which functions will be affected doing so.



5.1 SDRAM SELECTION

The board comes with a 32 MByte external SDRAM which is soldered on the board but by default disconnected from the RA6M3. In order to connect this device, multiple Shunts must be removed and soldered to switch from the **Default** board to the **SDRAM Ready** version. The following sections will describe you how to carry this out step by step. [Figure 29](#) shows you where to quickly find all the shunts related to the SDRAM.

[Figure 29. Shunt general location](#)



For a detailed location of each shunt please refer to the PCB layout document page 12 here:
https://www.m13design.fr/download/pdf/M13design_M13-RA6M3-EK_Schematic.pdf

5.1.1 DATA / SPI0

The first series of shunts to remove/solder will connect the DQ00-DQ04 signals to the RA6M3. Doing so will disconnect the SPI0 bus from the mikroBUS™ and both PMOD connectors as detailed in [Table 50](#).

Table 50. Multiplexing SDRAM Data & SPI0

RA6M3 Pin	RA6M3 Pin Description	Selected Function	Shunt to remove	Shunt to solder	Deactivated Function
132	P100 / MISOA_A / DQ00	DQ00	SH1	SH2	SPI0
131	P101 / MOSIA_A / DQ01	DQ01	SH3	SH4	SPI0
130	P102 / RSPCKA_A / DQ02	DQ02	SH5	SH6	SPI0
129	P104 / SSLA1_A / DQ04	DQ04	SH7	SH8	SPI0
128	P105 / SSLA2_A / DQ05	DQ05	SH9	SH10	SPI0

5.1.2 ADDR / SSIE0

The next series of shunts to remove/solder will connect the A01 to A04 signals to the RA6M3. Doing so will disconnect the SSIE channel as detailed in [Table 51](#).

Table 51. Multiplexing SDRAM Addresses & SSIE0

RA6M3 Pin	RA6M3 Pin Description	Selected Function	Shunt to remove	Shunt to solder	Deactivated Function
93	P112 / SSIBCK0_B / A04	A04	SH13	SH14	SSIE0
94	P113 / SSILRCK0 / A03	A03	SH15	SH16	SSIE0
95	P114 / SSIRXD0_B / A02	A02	SH17	SH18	SSIE0
96	P115 / SSITXD0_B / A01	A01	SH19	SH20	SSIE0

5.1.3 ADDR / SCI2

The next series of shunts to remove/solder will connect the A06 & A07 signals to the RA6M3. This will disconnect the UART channel (SCI2) of the mikroBUS™ connector as detailed in [Table 52](#).

Table 52. Multiplexing SDRAM Addresses & SCI2

RA6M3 Pin	RA6M3 Pin Description	Selected Function	Shunt to remove	Shunt to solder	Deactivated Function
87	P301 / RXD2 / A06	A06	SH21	SH22	SCI2
86	P302 / TXD2 / A07	A07	SH23	SH24	SCI2

5.1.4 ADDR / SCI6

The next series of shunts to remove/solder will connect the A09 & A10 signals to the RA6M3. This will thus disconnect the SCI6 channel as detailed in [Table 53](#).

Table 53. Multiplexing SC6 & SDRAM Addresses

RA6M3 Pin	RA6M3 Pin Description	Selected Function	Shunt to remove	Shunt to solder	Deactivated Function
82	P304 / SCL6 / A09	A09	SH25	SH26	SCI6
81	P305 / SDA6 / A10	A10	SH27	SH28	SCI6

Connecting the SDRAM signal A09 & A10 will deactivate the I²C interface from the MikroBUS™ and the PMOD1 connectors.

5.1.5 PMOD2

The last series of shunts to remove/solder before accessing the SDAM will connect the A05, DQM0 and the SDCLK signals to the RA6M3. This will remove the Reset functionality and the GPIOs on pin 9 and 10 from the PMOD2 Interface CN14 as detailed in [Table 54](#).

Table 54. Multiplexing PMOD_RST & SDRAM Address

RA6M3 Pin	RA6M3 Pin Description	Selected Function	Shunt to remove	Shunt to solder	Deactivated Function
92	P111 / RPMOD_RST / A05	A05	SH11	SH12	PMOD RST
121	P601 / RXD9 / DQM0	DQM0	SH29	SH30	PMOD IO9
120	P602 / TXD9 / SDCLK	SDCLK	SH31	SH32	PMOD IO10

5.1.6 “DEFAULT” AND “SDRAM READY” SHUNT CONFIGURATION RECAP

Table 55. Shunt Configuration Table 55 shows you the general view of the shunts to solder/remove to switch from the Default version of the board to the SDRAM Ready version.

Shunt reference	Default Version	SDRAM Ready Version
SH1	F ¹	DNF ²
SH2	DNF	F
SH3	F	DNF
SH4	DNF	F
SH5	F	DNF
SH6	DNF	F
SH7	F	DNF
SH8	DNF	F
SH9	F	DNF
SH10	DNF	F
SH11	F	DNF
SH12	DNF	F
SH13	F	DNF
SH14	DNF	F
SH15	F	DNF
SH16	DNF	F
SH17	F	DNF
SH18	DNF	F
SH19	F	DNF
SH20	DNF	F
SH21	F	DNF
SH22	DNF	F
SH23	F	DNF
SH24	DNF	F
SH25	F	DNF
SH26	DNF	F
SH27	F	DNF
SH28	DNF	F
SH29	F	DNF
SH30	DNF	F
SH31	F	DNF
SH32	DNF	F

Note1: F stands for Fitted (Soldered)

Note2: DNF stands for Do Not Fit (Not fitted / Not soldered)

Please note that the “Default” and the “SDRAM Ready” board versions are factory pre-soldered with the shunts described in Table 55. You are free to switch from either configuration manually if needed. M13design course will not be held responsible if the board is damaged during this process.

5.2 SD CARD / QSPI

The user has the possibility to either use the serial Flash memory U8 or the SD card connector CN10 multiplexed on PORT5 pin P500 to P505. This is done by shifting the jumper position on the JP3-JP8 Jumpers. [Figure 30, Table 56](#) shows you and describe you where and how to switch from the QSPI interface to the SDHI interface.

Figure 30. JP3 to JP8 Top location

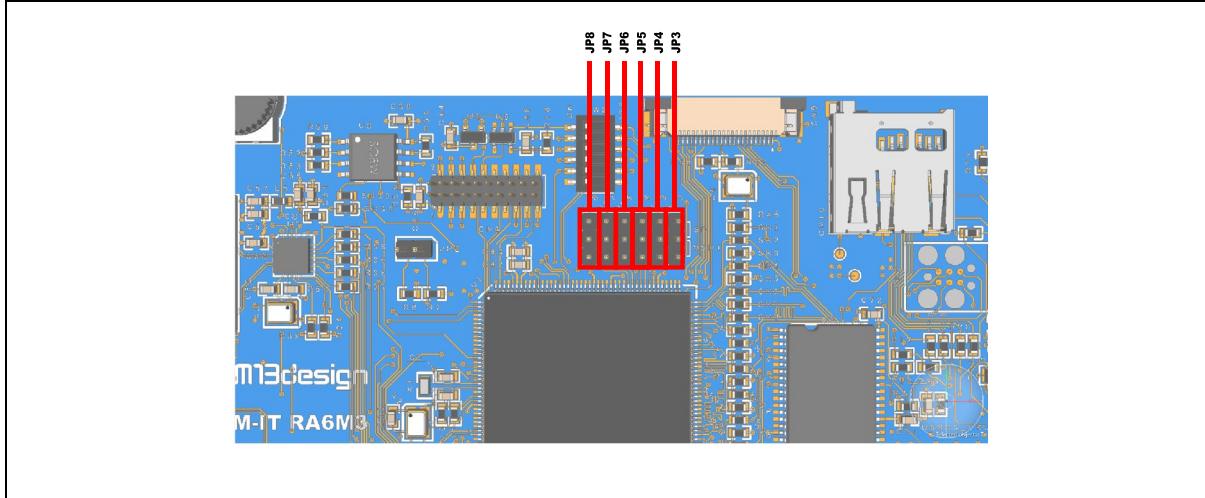


Table 56. QSPI/SDHI Selection

Jumper position view	Position Name (Displayed on PCB Silk)	Selected Function
JP8 JP7 JP6 JP5 JP4 JP3	QSPI	QSPI
JP8 JP7 JP6 JP5 JP4 JP3	SD	SDHI

5.3 TDI / CTS2 / IRQ11

As mentioned in Section [3.9 J-Link OB](#) the default debug protocol used on the board is SWD instead of TJAG. This gives us an extra GPIO P110 (which is used in JTAG configuration for the TDI signal) which is used for the mikroBUS™ interface on its pin 3 (CS with RTS capability). If needed, the user can switch to JTAG anytime by following the next instructions.

[Table 57](#) shows you which shunts to solder/remove in order to either map TDI or CTS2 on P110. And also, to rewire P708 to the mikroBUS™ connector in case you want to access the JTAG and the mikroBUS™ interface at the same time (Without CTS capability).

Table 57. Multiplexing TDI / CTS2 / IRQ11

RA6M3 Pin	RA6M3 Pin Description	Selected Function	SH33	SH34	SH35	SH36
91	P110 / CTS2 / TDI	TDI	F ¹	NF ²	NF	F
91	P110 / CTS2 / TDI	CTS2 ³	NF	F	F	NF
35	P708 / IRQ11	IRQ11	X ⁴	X	NF	F

Note 1: Fitted / Soldered / Shunted

Note 2: Not Fitted / Not Soldered / Removed

Note 3: CTS2 is selected by default

Note 4: Does not matter if Fitted or Not Fitted

5.4 SDA0_B / USB_VBUS

By default, the USBFS bus does not have VBUS monitoring capability. The user can access this function by following the instructions stated in [Table 58](#). Keep in mind that doing so, you will lose the I²C capability of the board's main I²C bus.

Table 58. Multiplexing SDA0_B & USB_VBUS

RA6M3 Pin	RA6M3 Pin Description	Selected Function	SH39	SH40
44	P407 / SDA0_B / USB_VBUS	SDA0_B ¹	F ²	NF ³
44	P407 / SDA0_B / USB_VBUS	USB_VBUS	NF	F

Note 1: Default configuration, SDA0_B is connected to the PMOD2 connector

Note 2: Fitted / Soldered / Shunted

Note 3: Not Fitted / Not Soldered / Removed

6 RELATED DOCUMENTS

Please find below the links to other hardware related documents for this evaluation board.

RA6M3 Datasheet
RA6M3 Schematic
RA6M3 PCB layout

https://www.m13design.fr/download/pdf/M13design_M13-RA6M3-EK_Datasheet.pdf
https://www.m13design.fr/download/pdf/M13design_M13-RA6M3-EK_Schematic.pdf
https://www.m13design.fr/download/pdf/M13design_M13-RA6M3-EK_PCB.pdf

Please refer to our product web page for any other information, here:

m13design.fr/products/M13-RA6M3-EK.html

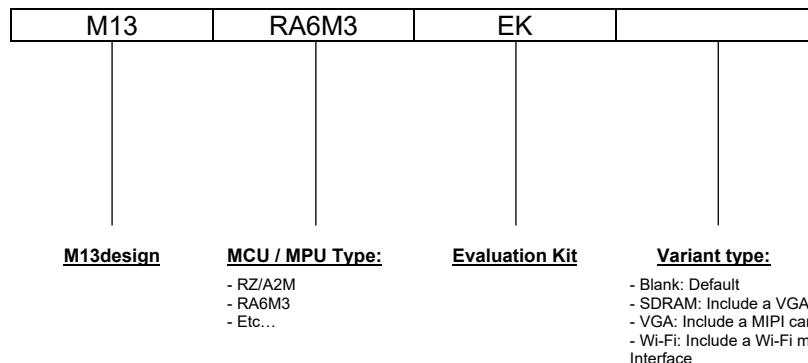
7 ORDERING INFORMATION

7.1 PART NUMBER DESCRIPTION

Table 59. Ordering Information

Part Number	Variant Type	Eval Board	SDRAM Ready ¹	TD7740 camera	MIKROE-2046
M13-RA6M3-EK	Default	✓	✗	✗	✗
M13- RA6M3-EK-SDRAM	SDRAM Camera	✓	✓	✗	✗
M13- RA6M3-EK-VGA	VGA Camera	✓	✗	✓	✗
M13- RA6M3-EK-WIFI	Wi-Fi Module	✓	✗	✗	✓

Note 1: SDRAM ready means the board is pre-soldered with the SDRAM's selection shunts as detailed in section [5.1.SDRAM Selection](#)



7.2 DEFAULT AND SDRAM-READY AVAILABLE FEATURES

[Table 60](#) shows you which board feature is available for each version of the board. The “VGA” and “Wi-Fi” Kit version are not mentioned in this table as they are actually the Default version with its respective accessory added to the kit as detailed in [Table 59](#).

Table 60. Default/SDRAM-Ready Features

Board Feature	Default version	SDRAM Ready
32 MByte external SDRAM	✗	✓
32 MByte external Serial Flash	✓	✓
16Kbit I ² C EEPROM	✓	✓
4.3-inch 480x272 TFT LCD with capacitive touch panel	✓	✓
USB Interface	✓	✓
LAN Interface	✓	✓
SD/MMC Host Interface (4 bits)	✓	✓
I ² S Audio codec	✓	✗
3-Axis accelerometer	✓	✓
8-bit Interface camera	✓	✓
microSD card	✓	✓
Mikrobus	✓	✗
PMOD1	✓	✗
PMOD2	✓	✗
User switch and Reset switch	✓	✓
Mono-turn 10KΩ Potentiometer	✓	✓
User LEDs	✓	✓
Power-on LED	✓	✓

8 TECHNOLOGY PARTNERS

Table 61. Hardware Technology Partners

Partners	Descriptions
	Renesas Electronics Corporation delivers trusted embedded design innovation with complete semiconductor solutions that enable billions of connected, intelligent devices to enhance the way people work and live. A global leader in microcontrollers, analog, power, and SoC products, Renesas provides comprehensive solutions for a broad range of automotive, industrial, infrastructure, and IoT applications that help shape a limitless future.
	Würth Elektronik eiSos is one of the leading manufacturers of electronic and electromechanical components in Europe. The product portfolio includes: EMC Components, EMC Filters, Capacitors, Inductors, RF Inductors and LTCC Components, Resistors, Quartz, Oscillators, Transformers, Components for Circuit Protection, Power Modules, LEDs, Connectors, Switches, High-Power Contacts, Assembly Technique, Wireless Connectivity and Sensors.

Table 62. Software Technology Partners

Partners	Descriptions
	Cynetics offers a range of innovative solutions for software design and development of embedded systems. Our portfolio includes ARM Cortex-M MCU and RTOS training classes, professional-grade middleware components (TCP/IP, SSL/TLS, SSH, GUI libraries, File Systems...) as well as world class embedded software tools (IDE, Debugger, JTAG/SWD & TRACE probes). For high-end embedded systems based on ARM Cortex-A MPUs, Cynetics promotes a broad range of System-on-Chips (SoC), Single Board Computers (SBC) and complete Human Machine Interfaces (HMI) targeting industrial, medical and vending machine markets. We also bring our expertise on both software (RTOS, Connectivity, Security, Embedded Linux) and hardware (ARM MCU/MPU) for a faster start of your embedded projects.
	Oryx Embedded offers a complete range of networking solutions for embedded systems, making the Internet of Things a reality. Our portfolio includes professional-grade TCP/IP components as well as SSL/TLS & SSH encryption to make your communications safe and secure.
	TES Electronic Solutions GmbH is an innovative technology and design services company offering intellectual properties (IP), embedded hard- and software for a vast range of customers in global markets, such as in industrial, automotive, consumer electronics, as well as in semiconductors. Key capabilities include embedded software, graphics, RF & antenna, radar, mixed-signal and digital ASIC and FPGA designs. Guiliani is a modern, powerful, intuitive and innovative C++ software framework for creating stylish Graphical User Interfaces on every embedded hardware. It is supported by best-in-class engineering services and time-proven in many millions of embedded systems. It is uniquely scalable and customizable to meet even demanding technical requirements. And it is also offered with flexible licensing to meet your commercial needs as well

9 REVISION HISTORY

Table 63. Revision Table

Revision	Date	Revision content
V1.0.0	22-Jan-21	- Initial release.
V1.0.0	26-Jan-21	- Added the section 6.Related documents
V1.0.1	03-Mar-21	<ul style="list-style-type: none"> - Updated Figure 4, Figure 5, Figure 6, Figure 8, Figure 11, Figure 14 & Figure 15. - Updated I²C information in section 3.2.3, 3.7, 3.8, 3.10, 3.11 - Added PMOD capability descriptions in section 4.11 - Modified the 5.Multiplexed Functions section
V1.0.2	06-Apr-21	<ul style="list-style-type: none"> - Updated Table 62. Software Technology Partners with TES Electronic Solutions / Giuliani - Added section 5.1.6. "Default" and "SDRAM ready" shunt Configuration recap - Updated the links in section 6.Related documents - Added section 7.Ordering information - Updated Table 62 with TES Electronic Solutions / Giuliani
V1.0.3	16-Dec-21	<ul style="list-style-type: none"> - Corrected PMOD2 pin 7 assignment information in Table 46 (From IRQ9 to IRQ10) - Corrected SCL0_B pin number in Table 12 / Table 23 / Table 25 - Updated headquarter address - Added TES / Giuliani in the 8.Technology Partners, Table 62

Disclaimer

Information in this document is subject to change without notice and does not represent a commitment on the part of the manufacturer. The software described in this document is provided under license and may only be used or copied in accordance with the terms of the agreement. It is illegal to copy the software onto any medium, except as specifically allowed in the licence or non-disclosure agreement.

No part of this manual may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying, recording, or information storage and retrieval systems, for any purpose without prior written permission. Every effort has been made to ensure the accuracy of this manual and to give appropriate credit to persons, companies and trademarks referenced herein. This manual exists in electronic form (pdf) only. Please check any printed version against the .pdf installed on the computer in the installation directory of the latest version of the software, for the most up-to-date version. The examples of code used in this document are for illustration purposes only and accuracy is not guaranteed. Please check the code before use.

Headquarters

M13DESIGN
165, rue Louis Barran
ZA Centr'Alp 2
38430 - Saint-Jean-de- Moirans – France

[/www.m13design.fr/](http://www.m13design.fr/)

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit or product web page:

www.m13design.fr/contact/