M13-RZ/A2M-EK

RZ/A2M (Cortex-A9)
Evaluation Kit

USER MANUAL

Board name:	**M13-RA6M3-EK**
MCU:	R7S921058VCBG
Version	1.0.2

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1 OVERVIEW

1.1 INTRODUCTION

The M13-RZ/A2M-EK is complete evaluation and development platform for the Renesas Electronics® based RZ/A2M Cortex®-A9 R7S921058VCBG microprocessor. The full range of the hardware features on the board helps users to quickly evaluate all the available peripherals (10/100-Mbit Ethernet, microSD™ card, USB host/device, Audio codec with 4-pole Jack, SDRAM, HyperRAM™ and HyperFlash™, Quad-SPI Flash memory,4.3-inch colour LCD-TFT with capacitive touch panel, and many others) and to develop their custom applications. PMOD™ and Mikrobus™ connectors make it possible to easily extent the boards features (Sensors, communication and network modules and many more). The integrated JLink-OB debug probe provides in-circuit debug and programming for the RZ/A2M device and also a built-in VCOM functionality.

Figure 1. M13-RZ/A2M-EK Component View

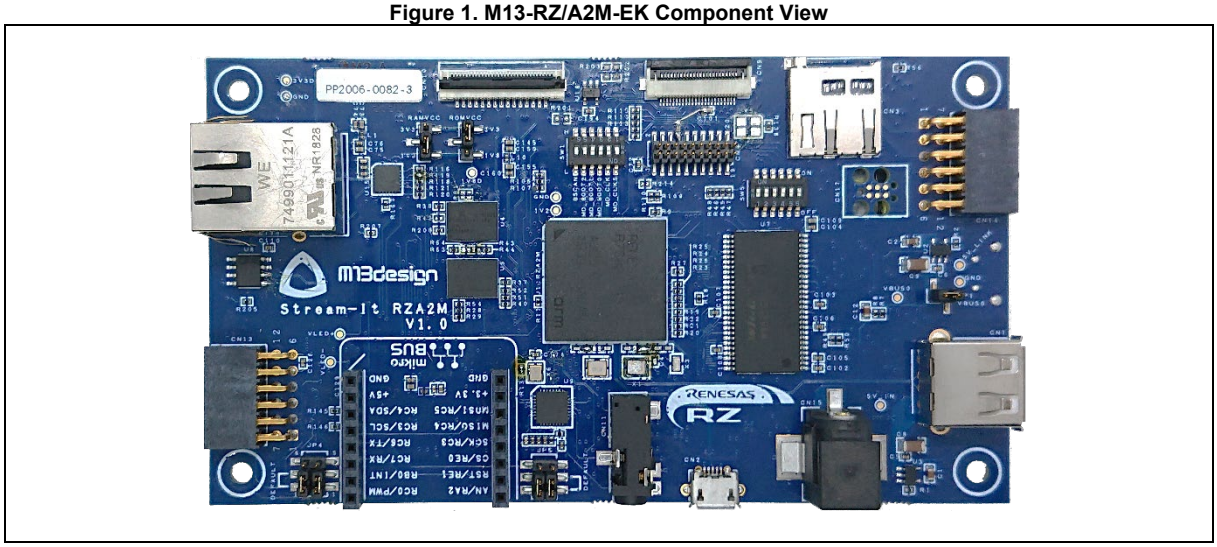
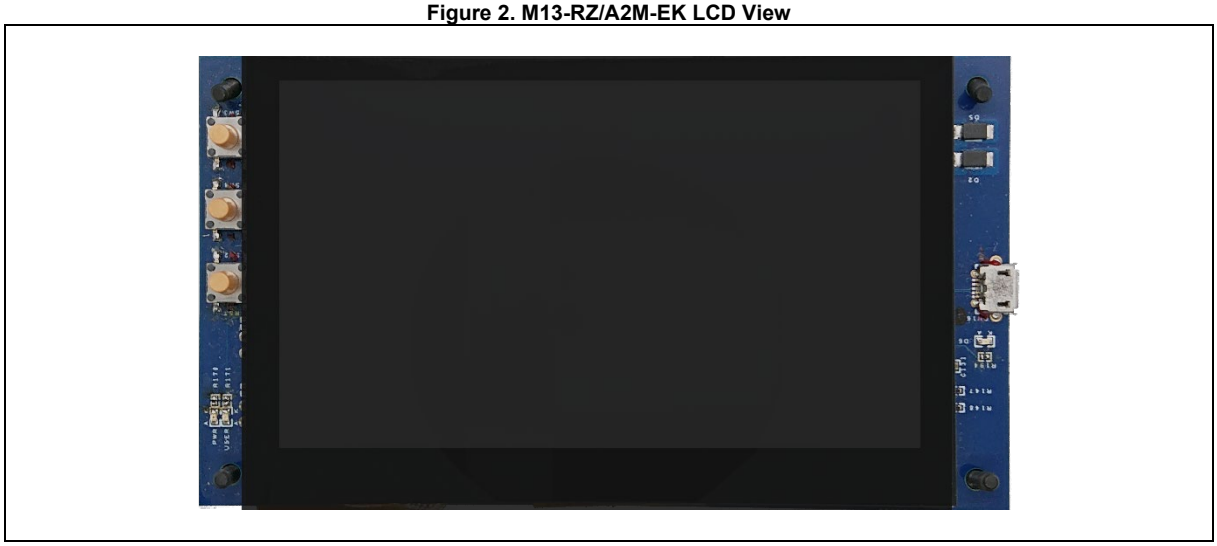


Figure 2. M13-RZ/A2M-EK LCD View



1.2 FEATURES

- Renesas RZ/A2M (Cortex®-A9) Microprocessor R7S921058VCBG
- 324-pins, 0.8mm-pitch BGA package
- 4 Mbyte Internal RAM
- 32 Mbyte external RAM
- 64 Mbyte external Serial Flash
- HyperMCP (Multi-Chip Package): 64MB HyperFlash™ and 8MB HyperRAM™ (1.8V)
- OctaRAM 64 MByte
- 16Kbit I2C EEPROM
- 4.3-inch 800x480 TFT LCD with capacitive touch panel
- USB Interface
- LAN Interface
- SD/MMC Host Interface (4 bits)
- I2S Audio codec
- 3-Axis accelerometer
- On-board JLINK-OB debugger with VCOM
- 19-pins 1.27mm pitch JTAG connector
- Board connectors
    - 1 x 8bit Interface camera
    - 1 x MIPI-CSI2 camera
    - 1 x Ethernet RJ45
    - 2 x USB Micro-AB
    - 1 x USB A-Type
    - 1 x microSD™ card
    - 1 x Mikrobus™
    - 2 x PMOD
    - 1 x 4-pole 3.5mm Jack
    - 1 x 2.1mm 5V Power Jack
- 2 x User switch and 1 x Reset switch
- 1 x Mono-turn 10KΩ Potentiometer
- 1 x User Led
- 1 x Power led

1.3 MEMORY MAPPING

Table 1 shows the RZ/A2M memory mapping of the **M13-RZ/A2M-EK**

Table 1. Memory mapping

Logical address	RZ/A2M Logical space	M13-RZ/A2M-EK Memory mapping
H'0000_0000	CS0 area: 64 MByte	
H'0400_0000	CS1 area: 64 MByte	
H'0800_0000	CS2 area: 64 MByte	
H'0C00_0000	CS3 area: 64 MByte	SDRAM: 32 MByte
H'0E00_0000		
H'1000_0000	CS4 area: 64 MByte	
H'1400_0000	CS5 area: 64 MByte	
H'1800_0000	Others: 128 MByte	
H'2000_0000	SPI multi I/O bus space: 256 MByte	Serial flash memory: 64 MByte
H'2400_0000		
H'3000_0000	HyperFlash space: 256 MByte	
H'3400_0000		
H'4000_0000	HyperRAM space: 256 MByte	
H'4080_0000		
H'5000_0000	OctaFlash space: 256 MByte	
H'6000_0000	OctaRAM space: 256 MByte	OctaRAM memory: 64 Mbyte
H'7000_0000	Reserved (cannot be used)	Reserved (cannot be used)
H'8000_0000	Large capacity internal RAM: 4 MByte	Large capacity internal RAM: 4 MByte
H'8040_0000	Others: 2044 MByte	Others: 2044 MByte
H'FFFF_FFFF		

2 HARDWARE LAYOUT AND CONFIGURATION

2.1 HARDWARE BLOCK DIAGRAM

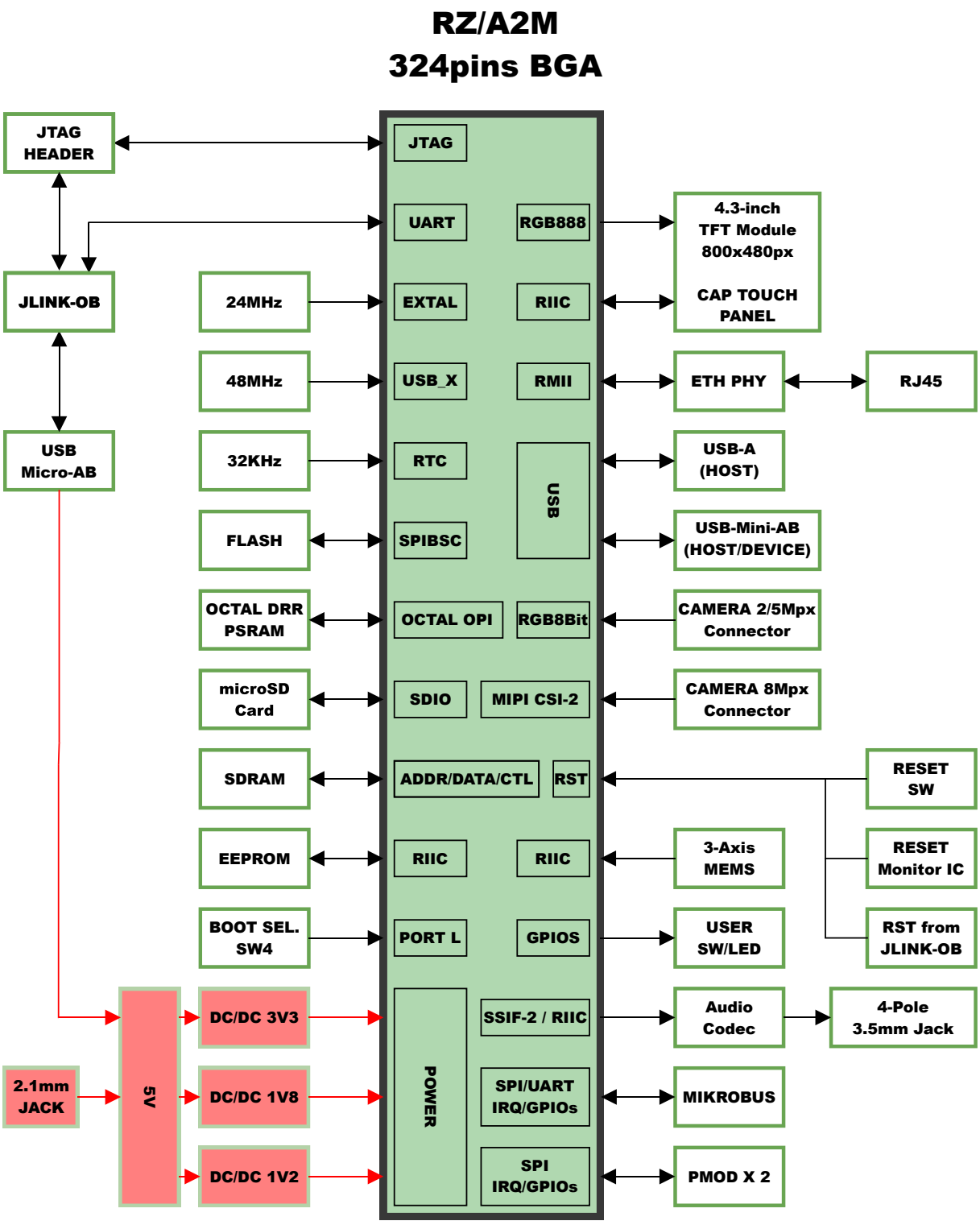


Figure 3. Bloc Diagram

2.2 THE M13-RZ/A2M-EK BOARD LAYOUT

Figure 4 and Figure 5 Show the layout of the main components of the board.

Figure 4. Top main component Layout

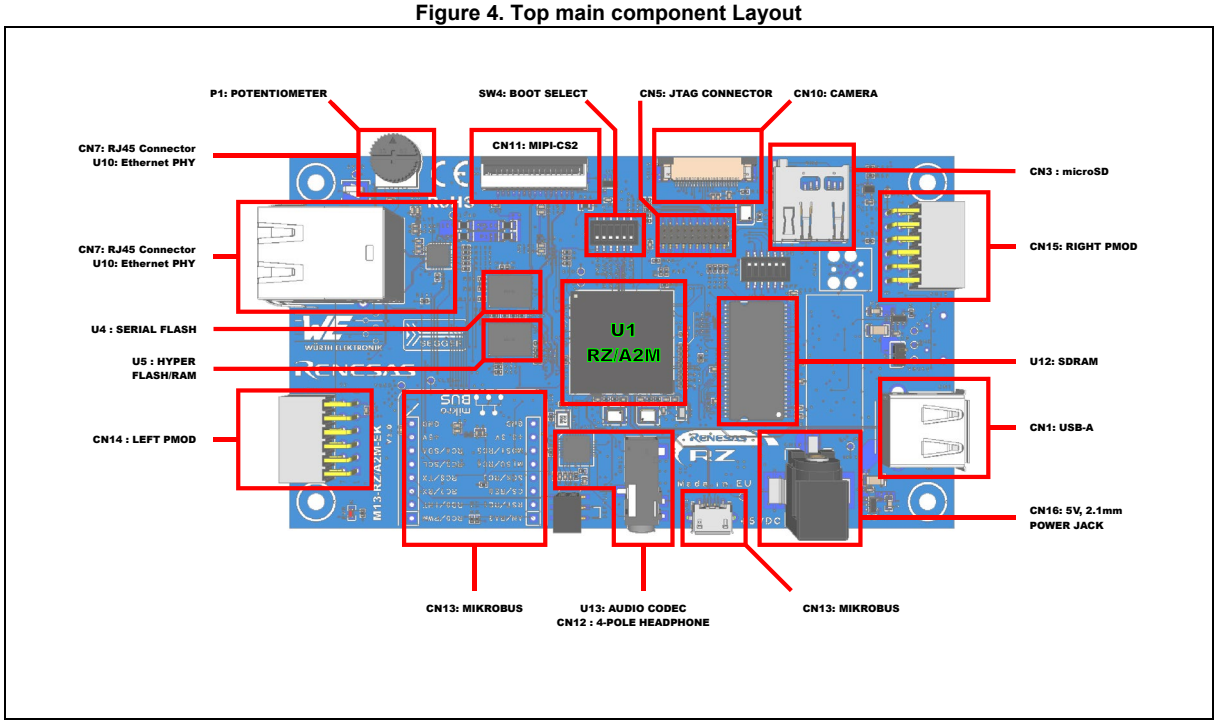


Figure 5. Bottom main component layout (Bottom view)

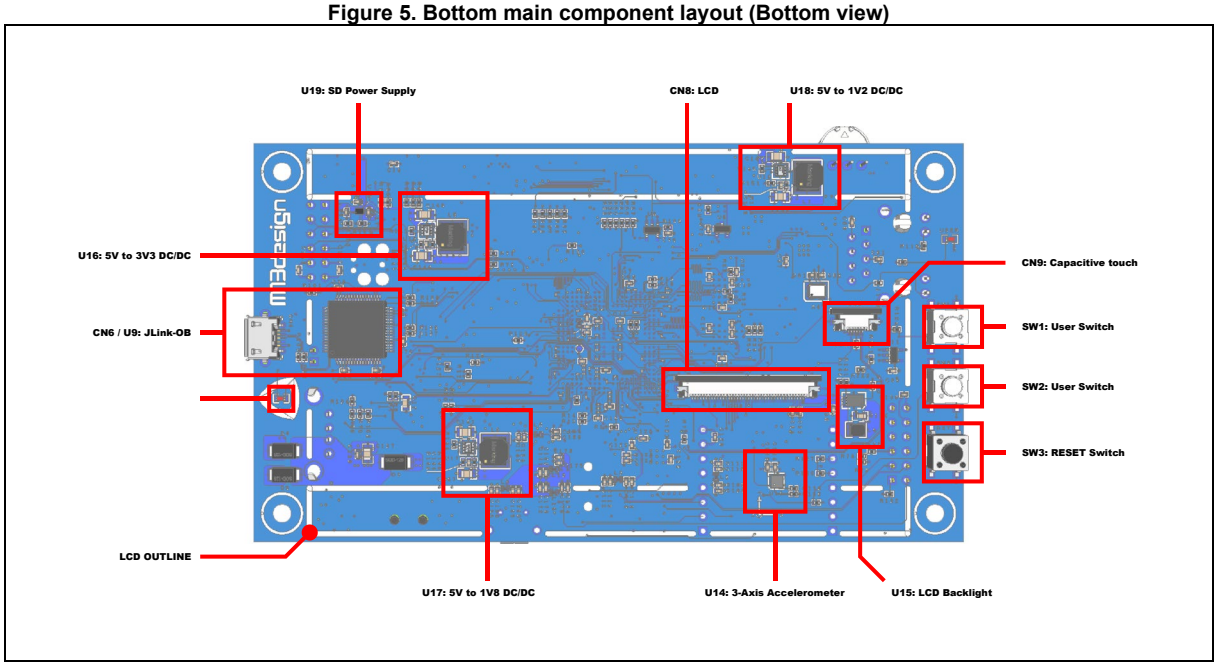


Table 2 And Table 3 list the main component mounted on the M13-RZ/A2M-EK board

Table 2. Top main component list

Component Reference	Description	MFR[1] / MPN[2]	NOTES
U1	CPU	Renesas / R7S921058VCBG	
U4	Serial Flash Memory	Macronix / MX25L51245GXDI-08G	
U5	HyperMCP	Cypress / S71KS512SC0BHV000	Combo Hyper Flash Hyper RAM
U12	SDRAM	Winbond / W9825G6KH-6I	
U10	Ethernet PHY	Microchip / KSZ8081RNA	
CN7	RJ45 connector	Würth Electronik / 7499011121A	
U13	Audio Codec	Maxim / MAX9867ETJ	
CN12	4-pole 3.5mm Jack headphone	Cui Inc. / SJ-43514-SMT-TR	
CN11	MIPI CSI-2	Würth Electronik / 686115148922	bottom contact
CN14	PMOD1	Würth Electronik / 613012243121	
CN13	Mikrobus	Würth Electronik / 61300811821	CN13.1 and CN13.2
CN16	5V, 2.1mm, Power Jack	Würth Electronik / 694106105102	Strictly 5VDC
CN5	19pins JTAG connector	Würth Electronik / 62102021021	1.27mm Pitch
CN3	Micro SD Card	Würth Electronik / 693071010811	
CN15	PMOD2	Würth Electronik / 613012243121	
CN1	USB-A	Würth Electronik / 61400416021	USB Host
SW4	Boot Select	Omron / A6H-6101	

Table 3. Bottom main component list

Component Reference	Description	MFR[1] / MPN[2]	NOTES
NA	LCD module	EastRising / ER-TFT043-7	From BuyDisplay
CN8	LCD connector	Würth Electronik / 687140183722	Bottom contact
CN9	Capacitive Touch connector	Würth Electronik / 687106183722	
U15	LCD Backlight	Renesas / ISL97634IRT26Z-T	
U9	JLink-OB	Segger	
CN6	Micro USB AB	Würth Electronik / 629105150921	JLink-OB connector
U16	3V3 DC/DC regulator	Renesas / ISL80030AFRZ-T7A	
U17	1V8 DC/DC regulator	Renesas / ISL80020AFRZ-T7A	
U18	1V2 DC/DC regulator	Renesas / ISL80020AFRZ-T7A	
U14	3-Axis Accelerometer	Würth Electronik / 2533020201601	
SW1	User Switch 1	C&K / KSC701JLFS	Blue colour
SW2	User Switch 2	C&K / KSC701JLFS	Blue colour
SW3	Reset Switch	C&K / KSC321JLFS	Black colour

Note 1: Manufacturer name
Note 2: Manufacturer Part Number

3 M13-RZ/A2M-EK PIN ASSIGNMENT

3.1 RZ/A2M SYSTEM AND POWER PINS

3.1.1 BOOT PINS

Table 4. Boot pins

U1 Pin	Pin Functions	Board Assignment	Signal Name	Function ID#	Remarks
A11	PL_2 / MD_B00T2 / IRQ6	Boot	MD_BOOT2	Mode Function	
B11	PL_3 / MD_B00T1 / IRQ7	Boot	MD_BOOT1	Mode Function	
C11	PL_4 / MD_B00T0 / IRQ0	Boot	MD_BOOT0	Mode Function	

The pins PL_2, PL_3 and PL_4 are used for selecting the Boot Mode at power up. See section 5.1 SW4: Boot and Clock Select for a full description of the Boot Mode selection.

3.1.2 SYSTEM RESET PIN

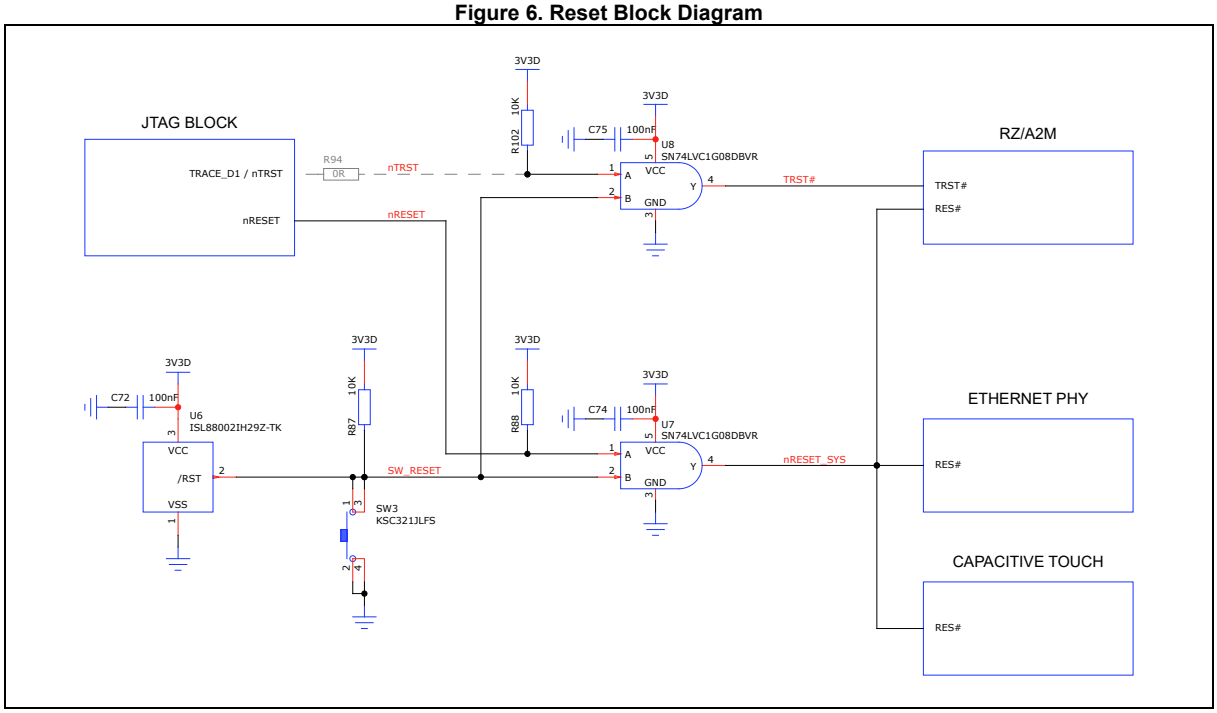
Table 5. System Reset pin

U1 Pin	RZ/A2M Pin Functions	Board Assignment	Signal Name	Function ID#	Remarks
AB9	RES#	Reset	nRESET_SYS	DF[1]	
F20	TRST#	TRST	TRST#	DF[1]	

Note 1: Dedicated Function

The **M13-RZ/A2M-EK** System reset signal is controlled by 3 sources: The power-on reset with the Voltage supervisor U6, the Reset Switch (SW3) and the JTAG reset signal. Figure 6 shows the reset block diagram. As a lack of free GPIO left, the system reset signal is also shared with the Ethernet PHY (U10) and the LCD's Capacitive Touch Device (CN9).

Figure 6. Reset Block Diagram



3.1.3 CLOCK SOURCE

The **M13-RZ/A2M-EK** has 3 clock input sources as shown in Figure 7.

- Main clock : 24MHz crystal
- USB clock : 48MHz crystal
- RTC clock : 32.768KHz crystal

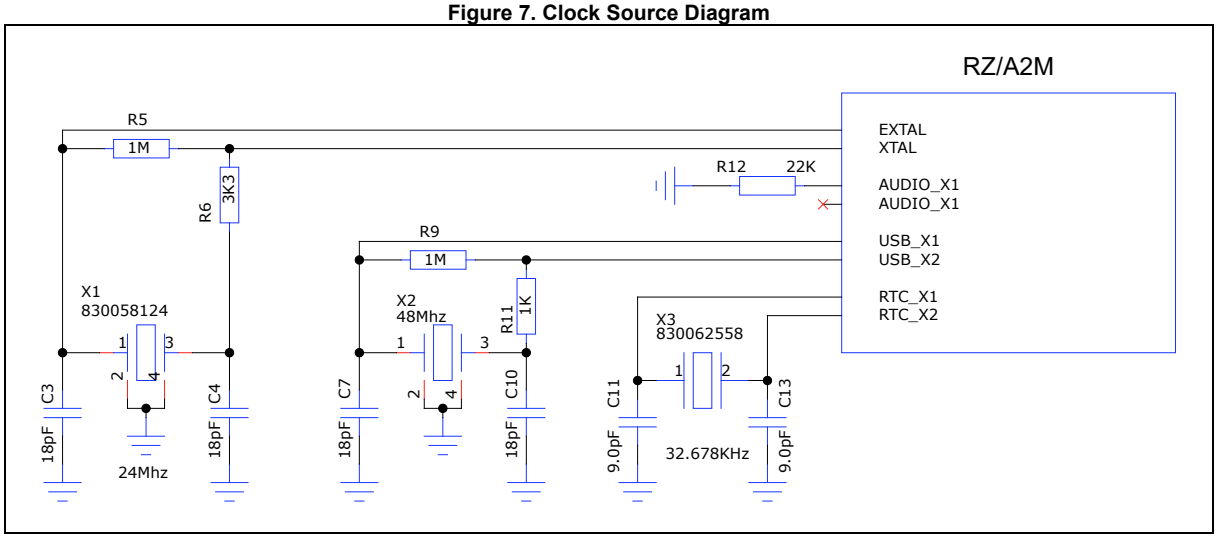
The Audio reference clock is not provided to the RZ/A2M, rather, it's provided directly to the Audio CODEC by an external source as shown in section 3.7 Audio Interface.

Table 6. Clock Source Assignment

U1 Pin	RZ/A2M Pin Functions	Board Function Assignment	Signal Name	Function ID#	Remarks
C12	PL_0 / MD_CLKS / IRQ4	Boot	MD_CLKS	Mode Function	
B12	PL_1 / MD_CLK / IRQ5	Boot	MD_CLK	Mode Function	
AB18	EXTAL	Main clock	EXTAL	DF[1]	
AA18	XTAL	Main clock	XTAL	DF[1]	
AB20	RTC_X1	RTC clock	RTC_X1	DF[1]	
AA20	RTC_X2	RTC clock	RTC_X2	DF[1]	
AB10	USB_X1	USB clock	USB_X1	DF[1]	
AA10	USB_X2	USB clock	USB_X2	DF[1]	
T1	AUDIO_X1	Not used	Not used	DF[1]	Pulled-down
T2	AUDIO_X2	Not used	Not used	DF[1]	Not connected

Note 1: Dedicated Function

Figure 7. Clock Source Diagram

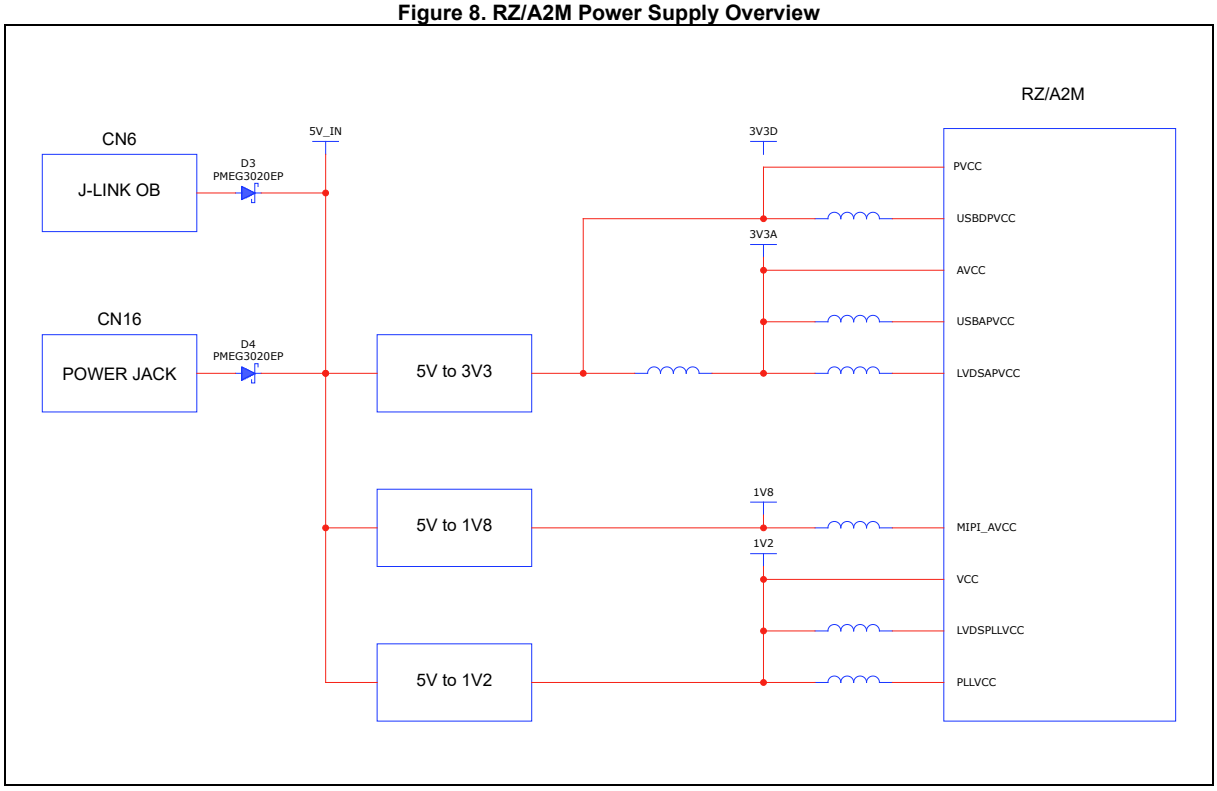


The pins PL_0 and PL_1 are respectively used for selecting the SSCG function and the EXTAL Clock range. See section 5.1 SW4: Boot and Clock Select for a full description of the Clock Configuration.

3.1.4 POWER SUPPLY

The **M13-RZ/A2M-EK** has 2 sources for its power supply. The Primary source is from the +5VDC/500mA of the J-Link OB USB connector CN6 as shown in Figure 8. The Secondary source is provided through the 2.10mm Power Jack connector CN16 and is strictly limited to a +5VDC power supply. Even though the power source is protected by diodes (D3 and D4) be extra cautious as to not provide the board's power from the Primary and the Secondary sources simultaneously.

Figure 8. RZ/A2M Power Supply Overview



3.2 EXTERNAL MEMORY

3.2.1 SERIAL FLASH MEMORY

The **M13-RZ/A2M-EK** board is equipped with a serial flash memory which is controlled by RZ/A2M on-chip SPI multi-I/O bus controller (SPIBSC). While in Boot Mode 3 (see section 5.1 SW4: Boot and Clock Select for full details on Boot Mode Selection), data will be read form the serial memory. Table 7 Shows the serial Flash Memory Overview.

Table 7. Serial Flash Memory Overview

Device Type	MFR[1] / MPN[2]	Operational Voltage	Capacity	Package
Serial Flash	Macronix / MX25L51245GXDI-08G	3.3V	64 Mbyte	BGA24 (6x8mm)

Table 8 Shows the pin assignment between the RZ/A2M MPU (U1) and the Serial Flash Memory (U4).

Table 8. Serial Flash Memory Pin Assignment

U1 Pin	RZ/A2M Pin Functions	Board Assignment	Signal Name	Function ID#	Remarks
A4	RPC_WP#	Not used	NA	DF[3]	Not connected
B7	QSPI0_SPCLK	QSPI	QSPI0_SPCLK	DF[3]	
C6	QSPI0_SSL	QSPI	QSPI0_SSL	DF[3]	
A3	QSPI1_SPCLK	QSPI	QSPI1_SPCLK	DF[3]	
C4	QSPI1_SSL	Not used	QSPI1_SSL	DF[3]	Pulled-up
C7	QSPI0_IO0	QSPI	ROM_D0	DF[3]	
B6	QSPI0_IO1	QSPI	ROM_D1	DF[3]	
D7	QSPI0_IO2	QSPI	ROM_D2	DF[3]	
A5	QSPI0_IO3	QSPI	ROM_D3	DF[3]	
B4	QSPI1_IO0	QSPI	ROM_D4	DF[3]	
B3	QSPI1_IO1	QSPI	ROM_D5	DF[3]	
D5	QSPI1_IO2	QSPI	ROM_D6	DF[3]	
A2	QSPI1_IO3	QSPI	ROM_D7	DF[3]	
C5	RPC_INT#	Not used	RPC_INT#	DF[3]	Pulled-up
B5	RPC_RESET#	QSPI	RPC_RESET#	DF[3]	

Through either R155 or R156, the Serial Flash Memory (U4) can by power supplied in 3.3V or 1.8V. Table 9 show the configurations for selecting the Serial Flash Memory power supply. The default power supply is 3.3V for the main variant of the board.

Table 9. Serial Flash Memory Power Setting

R155	R156	Power Supply
Fitted	Not fitted	1.8V
Not Fitted	Fitted	3.3V (Default)

Note 1: Manufacturer name
Note 2: Manufacturer Part Number
Note 3: Dedicated Function

3.2.2 OCTARAM

The **M13-RZ/A2M-EK** is equipped with an OctaRAM™ device from APMemory. This memory device is controlled by the RZ/A2M Octa Memory Controller. Table 10 Shows the details of the Memory device.

Table 10. OctaRAM Overview

Device Type	MFR[1] / MPN[2]	Operational Voltage	Capacity	Package
OctaRAM	AP Memory / APS51208N-OCH	1.8V	64 Mbyte	BGA24 (6x8mm)

Table 11 shows the pin assignment between the RZ/A2M MPU (U1) and the Memory device (U5).

Table 11. OctaRAM Pin assignment

U1 Pin	RZ/A2M Pin Functions	Board Assignment	Signal Name	Function ID#	Remarks
F3	HM_CK/OM_SCLK	Octa OPI	OM_SCLK	DF[3]	
F2	HM_CS0#/OM_CS0#	Octa OPI	OM_CS0#	DF[3]	
G3	HM_CS1#/OM_CS1#	Octa OPI	OM_CS1#	DF[3]	OctaRAM device
K3	PH_4 / HM_INT# / OM_ECS#	Octa OPI	OM_ECS#	Function 1	
J1	HM_RESET#/OM_RESET#	Octa OPI	OM_RESET#	DF[3]	
G2	HM_RWDS/OM_DQS	Octa OPI	OM_DQS	DF[3]	
H4	HM_DQ0/OM_SIO0	Octa OPI	OM_SIO0	DF[3]	
G1	HM_DQ1/OM_SIO1	Octa OPI	OM_SIO1	DF[3]	
H2	HM_DQ2/OM_SIO2	Octa OPI	OM_SIO2	DF[3]	
H3	HM_DQ3/OM_SIO3	Octa OPI	OM_SIO3	DF[3]	
H1	HM_DQ4/OM_SIO4	Octa OPI	OM_SIO4	DF[3]	
J4	HM_DQ5/OM_SIO5	Octa OPI	OM_SIO5	DF[3]	
J2	HM_DQ6/OM_SIO6	Octa OPI	OM_SIO6	DF[3]	
J3	HM_DQ7/OM_SIO7	Octa OPI	OM_SIO7	DF[3]	

Moreover, through either R157 or R158, the OctaRAM (U5) can by power supplied by either 3.3V or 1.8V. Table 12 show the configurations for selecting the power supply. The default power supply is 1.8V for the main variant of the board.

Table 12. OctaRAM Power Setting

R157	R158	Power Supply
Fitted	Not fitted	1.8V (Default)
Not Fitted	Fitted	3.3V

Note 1: Manufacturer name
Note 2: Manufacturer Part Number
Note 3: Dedicated Function

3.2.3 SDRAM

The **M13-RZ/A2M-EK** is also equipped with an external 16 bits SDRAM. This memory device is controlled by the RZ/A2M Bus State Controller. Table 13 shows the HyperMCP™ Memory Overview.

Table 13. SDRAM overview

Device Type	MFR[1] / MPN[2]	Operational Voltage	Capacity	Package
SDRAM	Winbond / W9825G6KH-6I	3.3V	32 Mbyte	TSOP54

Table 14 shows the pin assignment between the RZ/A2M and the SDRAM device.

Table 14. SDRAM Address Bus Pin Assignment

U1 Pin	RZ/A2M Pin Functions	Board Assignment	Signal Name	Function ID#	Remarks
D3	P8_1 / A1	SDRAM	A1	Function 1	
C2	P8_2 / A2	SDRAM	A2	Function 1	
B13	P8_3 / A3	SDRAM	A3	Function 1	
A13	P8_4 / A4	SDRAM	A4	Function 1	
C13	P8_5 / A5	SDRAM	A5	Function 1	
A14	P8_6 / A6	SDRAM	A6	Function 1	
B15	P8_7 / A7	SDRAM	A7	Function 1	
C15	P9_0 / A8	SDRAM	A8	Function 1	
A16	P9_1 / A09	SDRAM	A9	Function 1	
G22	P9_2 / A10	SDRAM	A10	Function 1	
H20	P9_3 / A11	SDRAM	A11	Function 1	
J19	P9_4 / A12	SDRAM	A12	Function 1	
H22	P9_5 / A13	SDRAM	A13	Function 1	
J22	P9_6 / A14	SDRAM	A14	Function 1	
K19	P9_7 / A15	SDRAM	A15	Function 1	
L3	P0_0 / D0	SDRAM	D0	Function 1	
L2	P0_1 / D1	SDRAM	D1	Function 1	
M1	P0_2 / D2	SDRAM	D2	Function 1	
M4	P0_3 / D3	SDRAM	D3	Function 1	
M3	P0_4 / D4	SDRAM	D4	Function 1	
M2	P0_5 / D5	SDRAM	D5	Function 1	
N3	P0_6 / D6	SDRAM	D6	Function 1	
W5	P1_0 / D7	SDRAM	D7	Function 1	
AA3	P1_1 / D8	SDRAM	D8	Function 1	
W6	P1_2 / D9	SDRAM	D9	Function 1	
AB4	P1_3 / D10	SDRAM	D10	Function 1	
Y5	P1_4 / D11	SDRAM	D11	Function 1	
W7	P2_0 / D12	SDRAM	D12	Function 1	
AB5	P2_1 / D13	SDRAM	D13	Function 1	
Y7	P2_2 / D14	SDRAM	D14	Function 1	
AB6	P2_3 / D15	SDRAM	D15	Function 1	
L20	P7_4 / CAS#	SDRAM	CAS#	Function 1	
K21	P7_5 / CKE	SDRAM	CKE	Function 1	
A21	CKIO	SDRAM	CKIO	DF[3]	
P21	P6_7 /WE0#/DQML	SDRAM	DQML	Function 1	
M21	P7_0 / WE1#/DQMU	SDRAM	DQMU	Function 1	
L21	P7_3 / RAS#	SDRAM	RAS#	Function 1	
L19	P7_1 / RD/WR#	SDRAM	RD/WR#	Function 1	
N19	P6_5 / CS3#	SDRAM	SDRAM_CS3#	Function 1	
L20	P7_4 / CAS#	SDRAM	CAS#	Function 1	

Note 1: Manufacturer name
Note 2: Manufacturer Part Number
Note 3: Default Function

3.2.4 EEPROM

An EEPROM is also available on the **M13-RZ/A2M-EK** board. This memory device is controlled by the RZ/A2M I2C bus on channel RIIC3. Table 15 shows the EEPROM Memory Overview.

Table 15. EEPROM Overview

Device Type	MFR[1] / MPN[2]	I2C Address	Capacity	Package
EEPROM	On Semiconductor / CAT24AA16TDI-GT3	W: 1010 0000 (0xA0) R: 1010 0001 (0xA1)	2048x8 bits (16Kbits)	TSOT-23-5

3.3 4.3-INCH TFT LCD MODULE

The 4.3-Inch TFT LCD module included in this kit is connected and controlled by the Video Display Controller 6 which output the video image in RGB888 format. The module comes with a Capacitive touchscreen as shown in Table 16. As for Table 18, it shows the assignment between the RZ/A2M and the TFT module.

Table 16. TFT LCD Module Overview

Device Type	MFR[1] / MPN[2]	Diagonal Size	Display Format	Package
TFT LCD Module	EastRising /ER-TFT043-7	4.3-Inch	800x480px	N/A

Table 17. Capacitive Touchscreen

Device Type	MFR[1] / MPN[2]	Diagonal Size	I2C Address	Package
Capacitive Touchscreen	EastRising / ER-TPC043-2	4.3-Inch	W: 0111 0000 (0x70) R: 0111 0001 (0x71)	N/A

Table 18. LCD Assignment Pins

U1 Pin	RZ/A2M Pin Functions	Board Assignment	Signal Name	Function ID#	ER-TFT043-7 pins
F4	PF_7 / LCD0_DATA0	LCD	LCD0_DATA0	Function 3	R0
C1	PH_2 / LCD0_DATA1	LCD	LCD0_DATA1	Function 3	R1
D9	PF_6 / LCD0_DATA2	LCD	LCD0_DATA2	Function 3	R2
B8	PF_5 / LCD0_DATA3	LCD	LCD0_DATA3	Function 3	R3
A9	PF_4 / LCD0_DATA4	LCD	LCD0_DATA4	Function 3	R4
D11	PF_3 / LCD0_DATA5	LCD	LCD0_DATA5	Function 3	R5
B14	PF_2 / LCD0_DATA6	LCD	LCD0_DATA6	Function 3	R6
C14	PF_1 / LCD0_DATA7	LCD	LCD0_DATA7	Function 3	R7
D14	PF_0 / LCD0_DATA8	LCD	LCD0_DATA8	Function 3	G0
D15	P8_0 / LCD0_DATA9	LCD	LCD0_DATA9	Function 3	G1
B17	PA_0 / LCD0_DATA10	LCD	LCD0_DATA10	Function 3	G2
D16	PA_1 / LCD0_DATA11	LCD	LCD0_DATA11	Function 3	G3
C17	PA_2 / LCD0_DATA12	LCD	LCD0_DATA12	Function 3	G4
B18	PA_3 / LCD0_DATA13	LCD	LCD0_DATA13	Function 3	G5
A20	PA_4 / LCD0_DATA14	LCD	LCD0_DATA14	Function 3	G6
B19	PA_5 / LCD0_DATA15	LCD	LCD0_DATA15	Function 3	G7
B20	PA_6 / LCD0_DATA16	LCD	LCD0_DATA16	Function 3	B0
D17	PA_7 / LCD0_DATA17	LCD	LCD0_DATA17	Function 3	B1
C19	PB_0 / LCD0_DATA18	LCD	LCD0_DATA18	Function 3	B2
F22	PB_1 / LCD0_DATA19	LCD	LCD0_DATA19	Function 3	B3
G20	PB_2 / LCD0_DATA20	LCD	LCD0_DATA20	Function 3	B4
G21	PB_3 / LCD0_DATA21	LCD	LCD0_DATA21	Function 3	B5
H19	PB_4 / LCD0_DATA22	LCD	LCD0_DATA22	Function 3	B6
H21	PB_5 / LCD0_DATA23	LCD	LCD0_DATA23	Function 3	B7
J20	P7_7 / LCD0_TC0N0	LCD	LCD0_TCON0	Function 3	DISP[4]
J21	P7_6 / LCD0_TC0N1	LCD	LCD0_TCON1	Function 3	HSYNC
L22	P7_2 / LCD0_TC0N2	LCD	LCD0_TCON2	Function 3	VSYNC
AA19	PC_4 / LCD0_TC0N3	LCD	LCD0_TCON3	Function 5[3]	DE[5]
K2	PJ_6 / LCD0_CLK	LCD	LCD0_CLK	Function 3	PLCK

Note 1: Manufacturer name
Note 2: Manufacturer Part Number
Note 3: Be careful as TCON3 is the only signal assigned on Function 5 as all the other pins are assigned on Function 3
Note 4: Display Enable, High-Level for “Display-on”, Low-Level for “Display-off”
Note 5: Data Enable

3.4 USB INTERFACE

The two USB channels available from the RZ/A2M are being used on this board. Channel 0 can be used either as a USB HOST or a USB DEVICE port, thus a Micro A/B connector type is being used. Channel 1 is used as a USB HOST-only port as we have equipped it with a Female USB Type-A connector.

When channel 0 is used as USB HOST, JP1 must be connected. On the other hand, leave it open if you want to use it as an USB DEVICE. Figure 9 illustrates the USB Interface general diagram while Table 20 gives you the RZ/A2M pin assignments.

Figure 9. USB Diagram

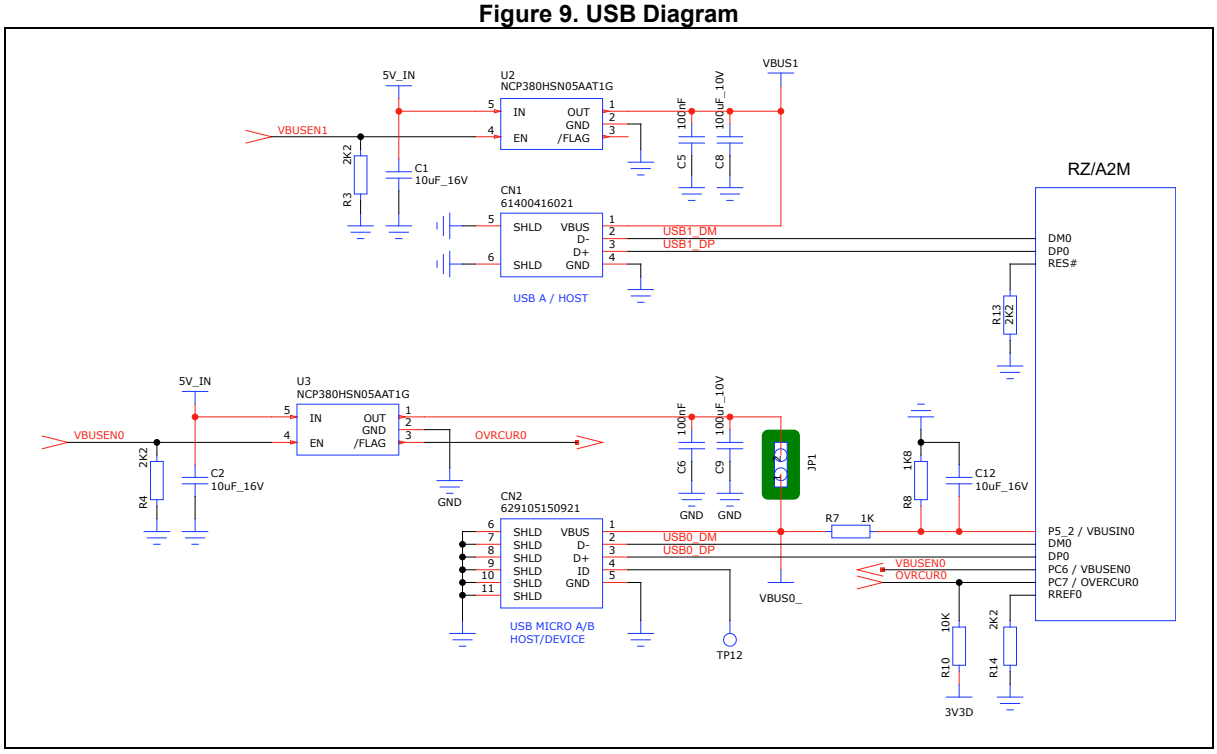


Table 19. USB Overview

Device Type	MFR[1] / MPN[2]	Package	Note
USB A-Type	Würth Electronik / 61400416021	TH[3], Right Angle	CN1
USB Mini A/B	Würth Electronik / 629105150921	SMD[4], Right Angle	CN2

Table 20. USB Pin Assignment

U1 Pin	RZ/A2M Pin Functions	Board Assignment	Signal Name	Function ID#	Note
AA13	RREF0	USB0	RREF0	DF[5]	2K2 Pull-down
AB13	DM0	USB0	USB0_DM	DF[5]	
AB11	DP0	USB0	USB0_DP	DF[5]	
AA11	PC_7 / OVRCUR0	USB0	OVRCUR0	Function 1	Pulled-up
AB15	PC_6 / VBUSEN0	USB0	VBUSEN0	Function 1	
AA15	P5_2 / VBUSIN0	USB0	VBUSIN0	Function 3	
Y17	RREF1	USB1	RREF1	DF[5]	2K2 Pull-down
Y18	DM1	USB1	USB1_DM	DF[5]	
AA17	DP1	USB1	USB1_DP	DF[5]	
W19	PC_5 / VBUSEN1	USB1	VBUSEN1	Function 1	

Note 1: Manufacturer name
Note 2: Manufacturer Part Number
Note 3: TH, Through Hole Device
Note 4: Surface Mount Device
Note 5: Default Function

3.5 LAN INTERFACE

The **M13-RZ/A2M-EK** embarks an Ethernet PHY (U10) which communicate through the RZ/A2M on-chip ethernet controller ETHERC channel 1 by using the RMII Interface. The details of this device can be seen in Table 21. As for the RMII pin assignment they are displayed in Table 22.

Table 21. Ethernet PHY Overview

Device Type	MFR[1] / MPN[2]	Operational Voltage	Bit Rate	Package
Ethernet PHY	Microchip / KSZ8081RNA	3.3V	10 Mbps / 100 Mbps	N/A

Note 1: Manufacturer name
Note 2: Manufacturer Part Number

Table 22. Ethernet Assignment Pins

U1 Pin	RZ/A2M Pin Functions	Board Assignment	Signal Name	Function ID#	Remarks
AA5	P3_0 / IRQ3	IRQ3	ET1_IRQ3	Function 5	
Y4	P3_3 / ET1_MDC	Ethernet	ET1_MDC	Function 1	
AA4	P3_4 / ET1_MDIO	Ethernet	ET1_MDIO	Function 1	
E3	PK_3 / REF50CK1	Ethernet	REF50CK1	Function 7	
T4	P3_2 / RMII1_CRS_DV	Ethernet	RMII1_CRS_DV	Function 7	
U2	PK_4 / RMII1_RXD0	Ethernet	RMII1_RXD0	Function 7	
T3	P3_5 / RMII1_RXD1	Ethernet	RMII1_RXD1	Function 7	
D8	PK_0 / RMII1_TXD_EN	Ethernet	RMII1_TXD_EN	Function 7	
B1	PK_1 / RMII1_TXD0	Ethernet	RMII1_TXD0	Function 7	
E4	PK_2 / RMII1_TXD1	Ethernet	RMII1_TXD1	Function 7	

3.6 SD/MMC HOST INTERFACE (4 BITS)

The **M13-RZ/A2M-EK** board embarks a microSD card connector which is connected to the RZ/A2M's SD/MMC Host Interface on channel 0 as shown in Figure 10 and Table 23. The 4 MSB bits of Channel 0 (SD0_DAT4 to SD0_DAT7) are not used and pulled-up. Channel 1 is not used and is left unconnected.

Figure 10.SD/MMC Host Interface Diagram

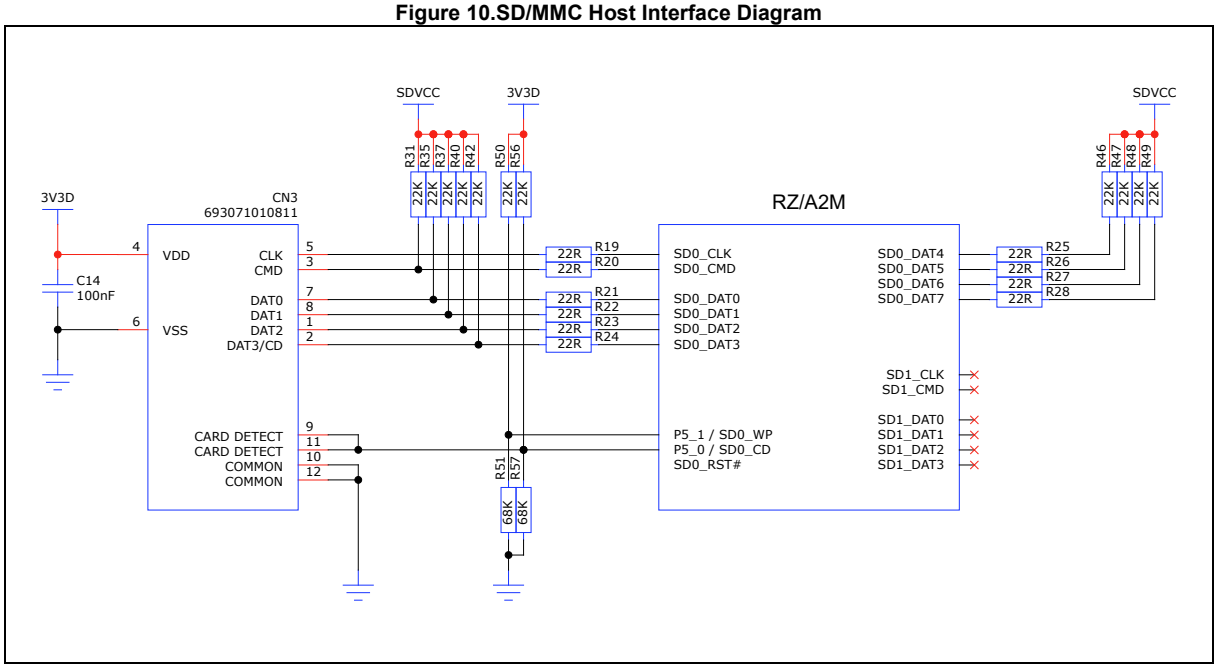


Table 23. SD/MMC Interface Pin Assignment

U1 Pin	RZ/A2M Pin Functions	Board Assignment	Signal Name	Function ID#	CN3 Pin
Y19	P5_0 / SD0_CD	Micro SD Card	SD0_CD	Function 3	9 & 11
Y20	P5_1 / SD0_WP	Micro SD Card	SD0_WP	Function 3	N/A
P3	PK_5	Micro SD Card	SDVCC_SEL	GPIO	N/A
U22	SD0_CLK	Micro SD Card	SD0_CLK	DF	5
U21	SD0_CMD	Micro SD Card	SD0_CMD	DF	3
T19	SD0_DAT0	Micro SD Card	SD0_DAT0	DF	7
T20	SD0_DAT1	Micro SD Card	SD0_DAT1	DF	8
R19	SD0_DAT2	Micro SD Card	SD0_DAT2	DF	1
T21	SD0_DAT3	Micro SD Card	SD0_DAT3	DF	2
R21	SD0_DAT4	Not used	N/A	DF	Pulled-up
R20	SD0_DAT5	Not used	N/A	DF	Pulled-up
R22	SD0_DAT6	Not used	N/A	DF	Pulled-up
P19	SD0_DAT7	Not used	N/A	DF	Pulled-up
P20	SD0_RST#	Not used	N/A	DF	Left not connected
Y22	SD1_CLK	Not used	N/A	DF	Left not connected
W21	SD1_CMD	Not used	N/A	DF	Left not connected
U19	SD1_DAT0	Not used	N/A	DF	Left not connected
V20	SD1_DAT1	Not used	N/A	DF	Left not connected
U20	SD1_DAT2	Not used	N/A	DF	Left not connected
V21	SD1_DAT3	Not used	N/A	DF	Left not connected

3.7 AUDIO INTERFACE

The **M13-RZ/A2M-EK** is equipped with a Maxim Audio CODEC (U13) for audio features. It's configurations and controls are done through the I2C interface using channel RIIC3. While the exchange of audio data is done using the Serial Sound Interface (SSIF-2) channel 1.

The output uses a single 4-pole 3.5mm audio jack connector for connecting a headset in single-ended mode. See section 4.10 CN12: 4-Pole Audio Jack for a detailed description on the headset configuration.

As the Audio CODEC is configurated and used in Master Mode, its operating clock is directly provided from an external 13MHz oscillator and not from the RZ/A2M. See Table 24 for the Audio CODEC details, Table 25 for its pin assignment and Figure 11 for a full illustration of the Audio Block Diagram.

Table 24. Audio CODEC Overview

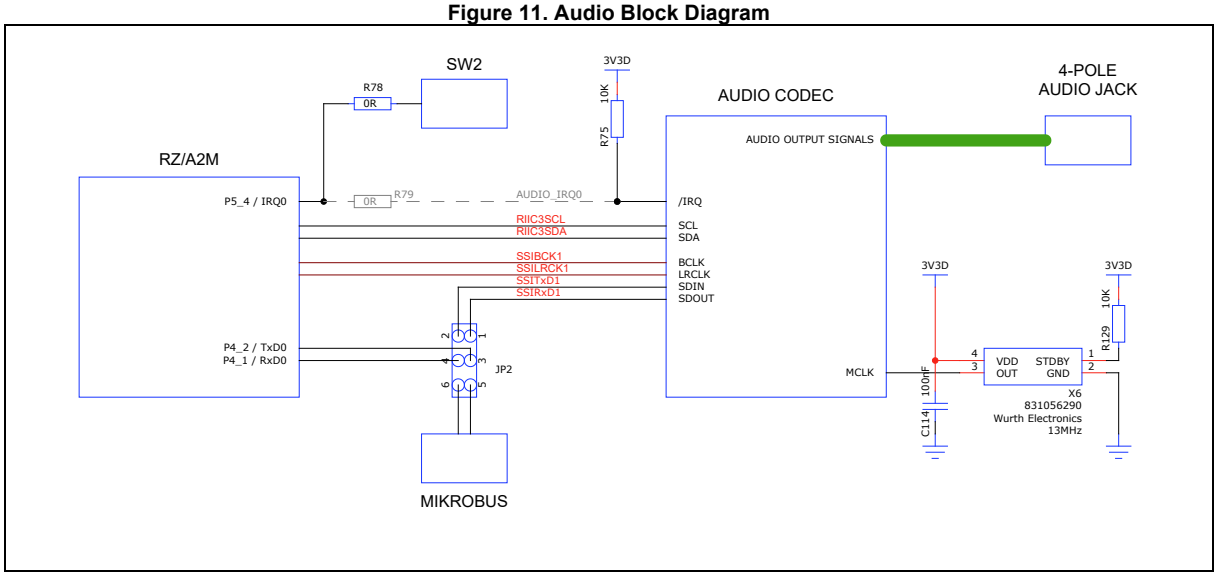
Device Type	MFR[1] / MPN[2]	Operational Voltage	I2C Address	Package
Audio CODEC	Maxim / MAX9867ETJ	1.8V	W: 0011 0000 (0x30) R: 0011 0001 (0x31)	QFN32

Table 25. Audio Pin Assignment

U1 Pin	RZ/A2M Pin Functions	Board Assignment	Signal Name	Function ID#	Remarks
AB7	P4_1 / SSIRxD1	SSIF-2	P4_1_RxD0[3]	Function 4	SSIRxD1
Y8	P4_2 / SSITxD1	SSIF-2	P4_2_TxD0[3]	Function 4	SSITxD1
V19	P5_4 / IRQ0	USER_SWITCH	P5_4[4]	GPIO	AUDIO_IRQ0
AA7	P4_0 / SSIBCK1	SSIF-2	SSIBCK1	Function 4	
W9	P4_3 / SSILRCK1	SSIF-2	SSILRCK1	Function 4	
D20	PD_6 / RIIC3SCL	I2C3	RIIC3SCL	Function 1	
C21	PD_7 / RIIC3SDA	I2C3	RIIC3SDA	Function 1	

Note 1: Manufacturer name
Note 2: Manufacturer Part Number
Note 3: The pins P4_1 and P4_2 are multiplexed with the Mikrobus™ Interface through Jumper JP2.
Note 4: The pin P5_4 is multiplexed with the User Switch SW2 through the configurations of R78 and R79.

Figure 11. Audio Block Diagram



See section 5.3. JP2: SCIFA Channel 0 Multiplexing for the configuration of the multiplexed GPIOs of the SSIF-2. And see also section 5.4. P5_4 Multiplexing for the settings of P5_4.

3.8 3-AXIS ACCELEROMETER

The **M13-RZ/A2M-EK** board is equipped with a 3-Axis Accelerometer. This device is controlled by the RZ/A2M I2C bus on channel RIIC2. Table 26 shows the device overview.

Table 26. Accelerometer Overview

Device Type	MFR[1] / MPN[2]	I2C Address	Scale	Package
MEMS	Würth Electronik / 2533020201601	W: 0011 0000 (0x32) R: 0011 0001 (0x33)	±2g, ±4g, ±8g, ±16g	LGA12 2.0x2.0x 0.7 mm

3.9 MIPI-CSI2 INTERFACE

The **M13-RZ/A2M-EK** board uses the available MIPI interface to connect a camera through the connector CN11. Table 28 shows the interface's pin assignments between the RZ/A2M and the CN11 connector.

Table 27.MIPI-CSI2 Interface Overview

Device Type	MFR[1] / MPN[2]	I2C Address	Package	Note
MIPI Camera	Raspberry / RPI-CAM-V2_1	W: 0010 0000 (0x20) R: 0010 0001 (0x21)		
Connector	Würth Electronik / 686115148922	N/A	SMD, 1.00mm 15 pin - Bottom contact	CN11

Table 28. MIPI-CSI2 assignment

U1 Pin	RZ/A2M Pin Functions	Board Assignment	Signal Name	Function ID#	CN11 Pin
V2	CSI_CLKN	MIPI-CSI2	CSI_CLKN	DF[3]	8
V1	CSI_CLKP	MIPI-CSI2	CSI_CLKP	DF[3]	9
W2	CSI_DATA0_N	MIPI-CSI2	CSI_DATA0N	DF[3]	2
W1	CSI_DATA0_P	MIPI-CSI2	CSI_DATA0P	DF[3]	3
Y2	CSI_DATA1_N	MIPI-CSI2	CSI_DATA1N	DF[3]	5
Y1	CSI_DATA1_P	MIPI-CSI2	CSI_DATA1P	DF[3]	6
M20	P6_0	MIPI_CAMERA	MIPI_CAM_EN	GPIO	11
D20	PD_6 / RIIC3SCL	I2C3	RIIC3SCL	Function 1	13
C21	PD_7 / RIIC3SDA	I2C3	RIIC3SDA	Function 1	14

Note 1: Manufacturer name
Note 2: Manufacturer Part Number
Note 3: Default Function

3.10 J-LINK OB

The **M13-RZ/A2M-EK** board embarks a J-Link OB from Segger, which is the board's default debugging and programming probe. The J-Link OB supports JTAG, SWD (+SWO) and one VCOM interface. Through its USB connector (CN6) the J-Link OB is also the board main 5VDC power supply.

Figure 12 illustrate the overall configuration of the debug interface of the board. And Table 29 shows you the detailed assignment between the RZ/A2M and the board for all the JTAG/SWD signals.

Figure 12. Debug Interface Diagram

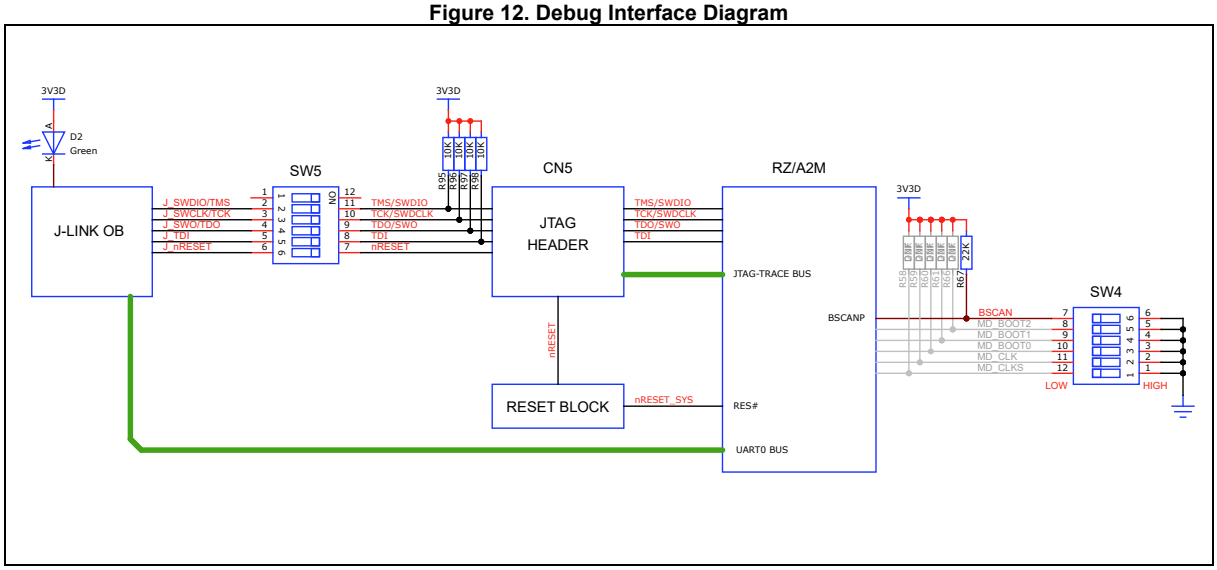


Table 29. JTAG Pin Assignment

U1 Pin	RZ/A2M Pin Functions	Board Assignment	Signal Name	Function ID#	Remarks
E21	TCK / SWDCLK	JTAG	TCK/SWDCLK	DF[1]	Pulled-up
E22	JP0_0 / TDI	JTAG	TDI	Function 1	Pulled-up
G19	JP0_1 / TD0 / SW0	JTAG	TDO/SWO	Function 1	Pulled-up
F21	TMS / SWDIO	JTAG	TMS/SWDIO	DF[1]	Pulled-up
F20	TRST#	JTAG	TRST#	DF[1]	
K4	PJ_0 / TRACECLK	JTAG_TRACE	PJ_0	Function 1	TRACE_CLK
N4	PJ_2 / TRACE_DATA0	JTAG_TRACE	PJ_2	Function 1	TRACE_D0
N1	PJ_3 / TRACE_DATA1	JTAG_TRACE	PJ_3	Function 1	TRACE_D1
R2	PJ_4 / TRACE_DATA2	JTAG_TRACE	PJ_4	Function 1	TRACE_D2
R3	PJ_5 / TRACE_DATA3	JTAG_TRACE	PJ_5	Function 1	TRACE_D3
AB8	P4_5 / RxD4	VCOM	RxD4	Function 4	
Y9	P4_6 / TxD4	VCOM	TxD4	Function 4	

Note 1: Dedicated Function

The reset signal from the J-Link OB is not detailed in this section. You will find a complete description of this signal in section 3.1.2.System Reset pin.

While assuming you already have the J-Link OB probe drivers installed, Table 30 shows you the configurations and status for using the on-board debugger or if needed other third-party ones.

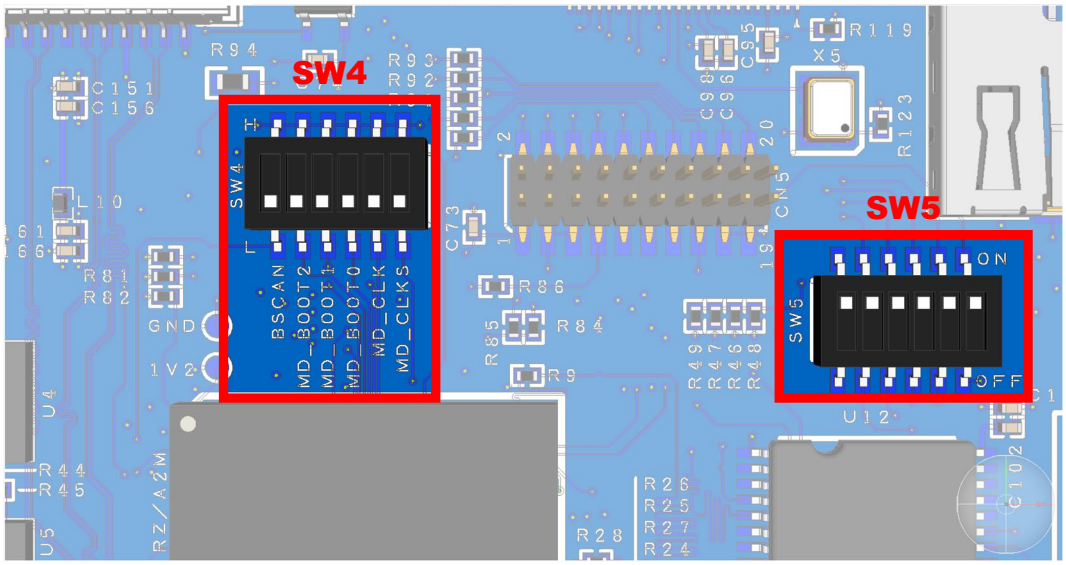
Table 30. Debug Configuration

Probe used for debug	SW5.2 to SW5.6	SW4.6	D2 (Status Led)
J-Link OB (Default)	On	L	Turned on
External JTAG Probe (With Trace)	Off	L	Blinking[2]
External Boundary Probe	Off	H	Blinking[2]

Note 2: D2 will keep blinking until the J-Link OB is connected to a computer USB port through CN6

In order to use the J-Link OB, make sure to slide all the SW5 switches on the “On” position and that the slide switch for the BSCANP signal SW4.6 is switched on the “L” position. See Figure 13, which represents the PCB Top Silkscreen, to have a better visualization of the “On/Off” and the “L/H” position respectively for SW4 and SW5.

Figure 13. SW4 and SW5 Illustration



In addition, if the use of an external probe is desired, make sure all the levers of SW5 are switched on the “Off” position. This will disconnect the J-Link OB from the JTAG/SWD bus thus avoiding any potential conflicts while using an external probe. See 5.2 SW5: J-Link OB Disconnection switch for a full graphic description of SW5.

3.11 VGA CAMERA MODULE

The **M13-RZ/A2M-EK** board is also capable to drive VGA camera modules with its Capture Engine Unit. Through the connector CN10, we provide an 8-bit interface which is compatible with many modules actually on the market. Table 32 shows the RZ/A2M pin assignments. For details on the connector, see 4.8 CN10: 8 Bit VGA Camera module**.**

Table 31. VGA Camera Module Overview

Device Type	MFR[1] / MPN[2]	I2C Address	Package	Note
VGA Camera	TD Next / TD7740	W: 0010 0000 (0x42) R: 0010 0001 (0x43)	N/A	
Connector	Würth Electronik / 68712414022	N/A	SMD, 0.50mm Right angle 24 pin - Top contact	CN10

Table 32. 8bit VGA Interface Pin Assignment

U1 Pin	RZ/A2M Pin Functions	Board Assignment	Signal Name	Function ID#	CN10 Pin
P2	PH_5	Camera	CAM_PWR_DN	GPIO	8
P1	PH_6	Camera	CAM_RST	GPIO	6
C8	P6_1 / VIO_CLK	Camera	VIO_CLK	Function 2	17
C10	PH_1 / VIO_D0	Camera	VIO_D0	Function 2	19
B10	PH_0 / VIO_D1	Camera	VIO_D1	Function 2	21
A10	PE_6 / VIO_D2	Camera	VIO_D2	Function 2	22
A12	PE_5 / VIO_D3	Camera	VIO_D3	Function 2	20
A15	PE_4 / VIO_D4	Camera	VIO_D4	Function 2	18
B16	PE_3 / VIO_D5	Camera	VIO_D5	Function 2	16
C16	PE_2 / VIO_D6	Camera	VIO_D6	Function 2	14
A19	PE_1 / VIO_D7	Camera	VIO_D7	Function 2	12
B9	P6_3 / VIO_HD	Camera	VIO_HD	Function 2	9
C9	P6_2 / VIO_VD	Camera	VIO_VD	Function 2	7
D20	PD_6 / RIIC3SCL	I2C3	RIIC3SCL	Function 1	5
C21	PD_7 / RIIC3SDA	I2C3	RIIC3SDA	Function 1	3

3.12 USER INTERFACE: SWITCH AND LED

The **M13-RZ/A2M-EK** board contains 2 User Switches and one User Led (Green coloured) as described in Table 34.

Table 33. User Interface Overview

Device Type	MFR[1] / MPN[2]	REFERENCE	Package	Note
User Switch	C&K / KSC701JLFS	SW1	SMD, Top Switch	SW1
User Switch	C&K / KSC701JLFS	SW2	SMD, Top Switch	SW2
User Led	Wurth Electronics / 150060VS55040	D1	SMD D0603	D1

Table 34. User Interface Pin Assignment

U1 Pin	RZ/A2M Pin Functions	Board Assignment	Signal Name	Function ID#	Note
N2	PJ_1	USER_LED	PJ_1	GPIO	
V19	P5_4	USER_SWITCH	SW2	GPIO	Multiplexed[3] with AUDIO_IRQ0
D10	PE_0	USER_SWITCH	SW1	GPIO	

Note 1: Manufacturer name
Note 2: Manufacturer Part Number
Note 3: See Section 5.4 P5_4 Multiplexing for multiplexing details.

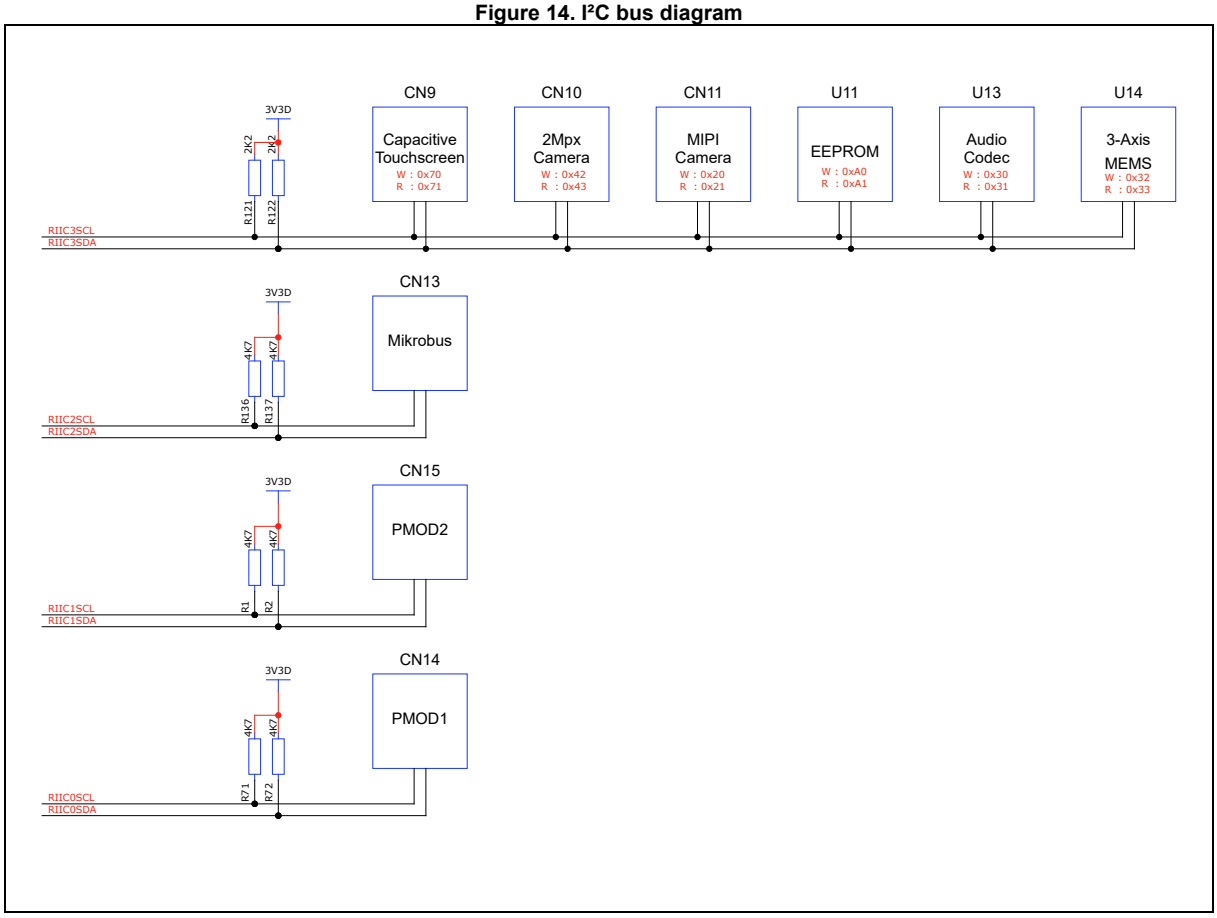
3.13 I2C INTERFACE

The **M13-RZ/A2M-EK** board uses all four I²C channel buses which the RZ/A2M has available. Table 35 shows you how each of these channels are mapped onto the board.

Table 35. I²C pin assignment

U1 Pin	RZ/A2M Pin Functions	Board Assignment	Signal Name	Function ID#	Remarks
F19	PD_0 / RIIC0SCL	I2C0	RIIC0SCL	Function 1	PMOD1
D22	PD_1 / RIIC0SDA	I2C0	RIIC0SDA	Function 1	PMOD1
E20	PD_2 / RIIC1SCL	I2C1	RIIC1SCL	Function 1	PMOD2
C22	PD_3 / RIIC1SDA	I2C1	RIIC1SDA	Function 1	PMOD2
D21	PD_4 / RIIC2SCL	I2C2	RIIC2SCL	Function 1	MikroBUS
E19	PD_5 / RIIC2SDA	I2C2	RIIC2SDA	Function 1	MikroBUS
D20	PD_6 / RIIC3SCL	I2C3	RIIC3SCL	Function 1	Main I²C bus
C21	PD_7 / RIIC3SDA	I2C3	RIIC3SDA	Function 1	Main I²C bus

Figure 14. I²C bus diagram



As illustrated in Figure 14 the channel 3 (RIIC3) is the board's main I²C bus. In addition, each expansion connector has been attributed with one bus. RIIC0 and RIIC1 channel signal names are not officially I²C specifically named as the PMOD protocol does not propose I²C interface. Rather, they are made available on the PMOD expansion connector in order to give the interface more flexibility.

4 CONNECTOR OVERVIEW

4.1 CN1: USB-A

Figure 15. CN1: USB-A Front view

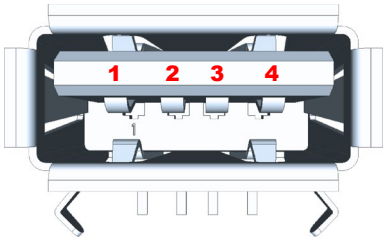


Table 36. CN1 Pin Description

CN1 Pin	Pin Description	Signal Name	RZ/A2M Pin	Note
1	VBUS	VBUS1	-	From U2.1
2	D-	USB1_DM	AB15	
3	D+	USB1_DP	AA15	
4	GND	GND	-	

4.2 CN2: USB-MICRO A/B: HOST/DEVICE

Figure 16. CN2: USB-micro-A/B Front view

Table 37. CN2 Pin Description

CN2 Pin	Pin Description	Signal Name	RZ/A2M Pin	Note
1	VBUS	VBUS0	-	From JP1
2	D-	USB0_DM	AB11	
3	D+	USB0_DP	AA11	
4	ID	Not used	-	
5	GND	GND	-	

4.3 CN3: MICRO SD CARD

Figure 17. CN3: MicroSD Card Bottom View

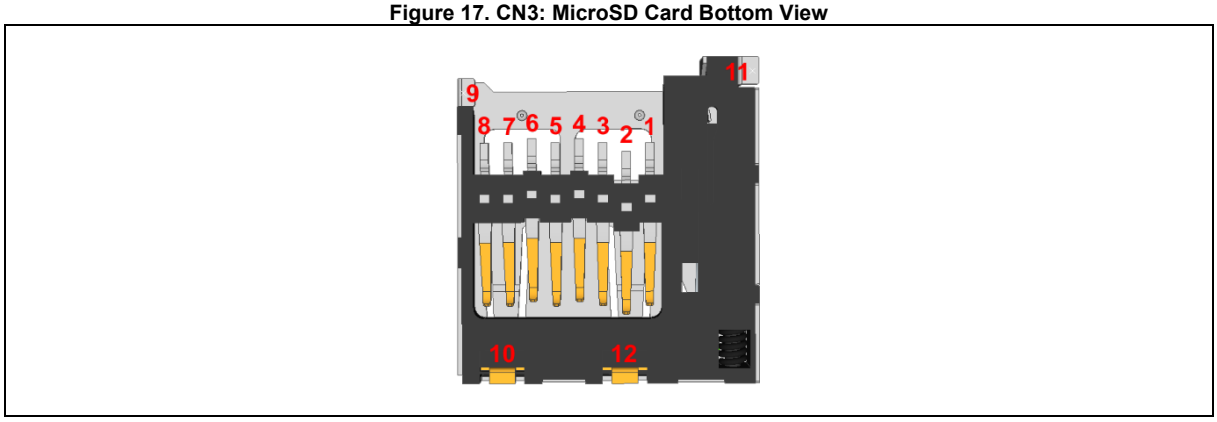


Table 38. CN3: Micro SD Card Pin Assignment

CN3 Pin	Pin Description	Signal Name	RZ/A2M Pin	Note
1	DAT2	SD0_DAT2	R19	
2	DAT3/CD	SD0_DAT3	T21	
3	CMD	SD0_CMD	U21	
4	VDD	3V3D	-	
5	CLK	SD0_CLK	U22	
6	VSS	GND	GND	
7	DAT0	SD0_DAT0	T19	
8	DAT1	SD0_DAT1	T20	
9 & 11	CARD DETECT	SD0_CD	Y19	
10 & 12	COMMON	GND	-	

4.4 CN5: 19-PIN JTAG HEADER

Figure 18. CN5: 19-pin JTAG Header

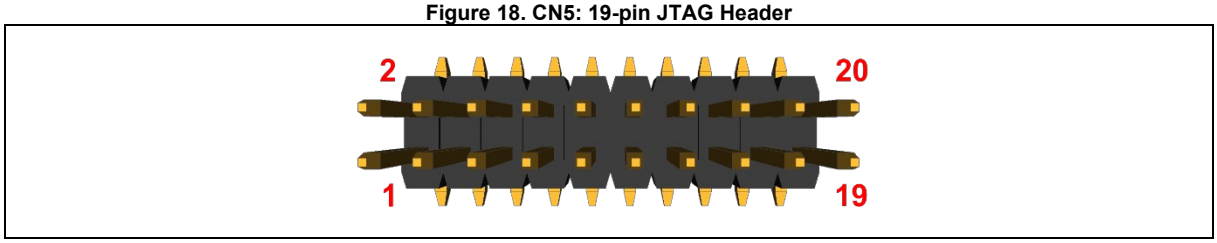


Table 39. CN5 Pin Assignment

CN5 Pin	Pin Description	Signal Name	RZ/A2M Pin	Note
1	VTREF	3V3D	N/A	
2	SWDIO/TMS	TMS/ SWDIO	F21	
3	GND	GND	-	
4	SWCLK/TCK	TCK/SWCLK	E21	
5	GND	GND	-	
6	SWO/TDO	TDO/SWO	G19	
7	-	BSCAN	D2	
8	TDI	TDI	E22	
9	NC	-	-	
10	nRESET	nRESET	-	
11	VCC	-	-	
12	TRACE_CLK	TRACE_CLK	K4	
13	VCC	-	-	
14	TRACE_D0	TRACE_D0	N4	
15	GND	GND	-	
16	TRACE_D1	TRACE_D1	N1	

Table 39. CN5 Pin Assignment (Continued)

CN3 Pin	CN3 Pin Description	Signal Name	RZ/A2M Pin	Note
17	GND	GND	-	
18	TRACE_D2	TRACE_D2	R2	
19	GND	GND	-	
20	TRACE_D3	TRACE_D3	R3	

4.5 CN7: RJ45

Figure 19. CN7. RJ45 Bottom View

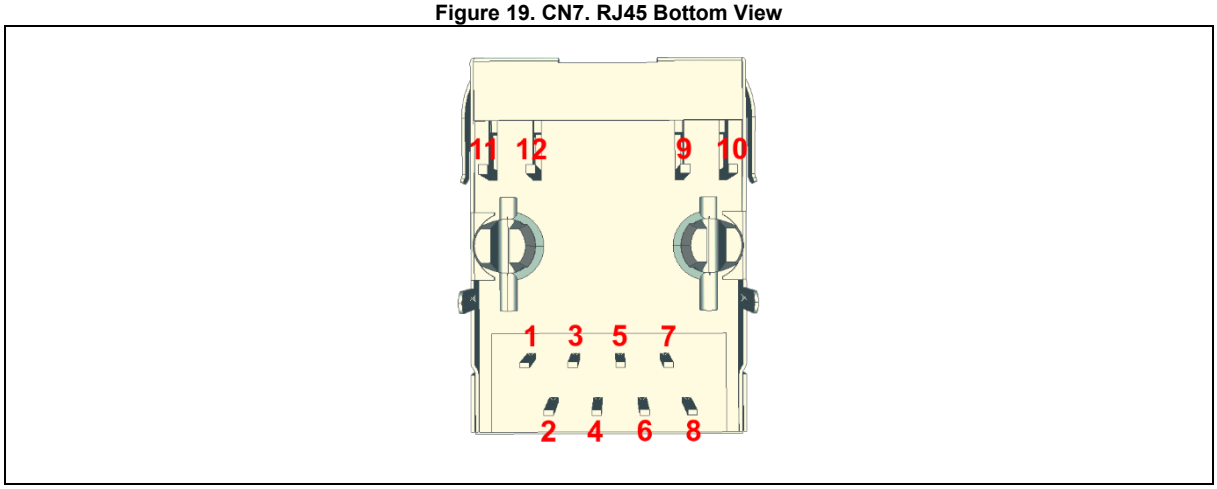


Table 40. CN7 Pin Assignment

CN7 Pin	Pin Description	Signal Name	U10 Pin	Note
1	TD+	TXP	6	
2	TCT	-	-	
3	TD-	TXM	5	
4	RD+	RXP	4	
5	RCT	-	-	
6	RD-	RXM	3	
7	NC	-	-	
8	COM	GND	-	
9	LED1+	3V3D	-	
10	LED1-	-	23	
11	LED2+	3V3D	-	
12	LED2-	-	-	Pulled-down

4.6 CN8: LCD CONNECTOR

Figure 20. CN8. Front View

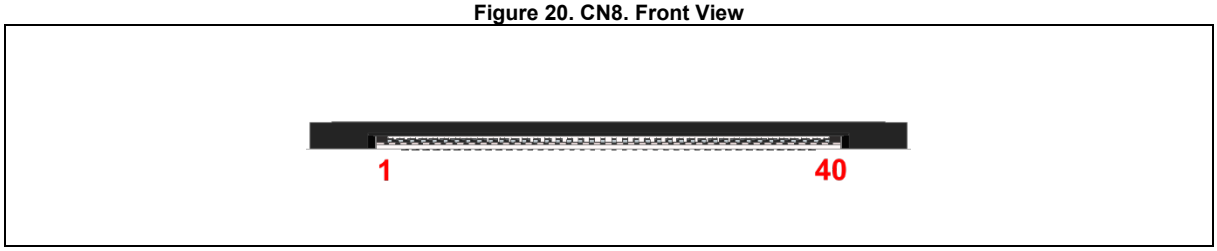


Table 41. CN8 Pin Assignment

CN8 Pin	Pin Description	Signal Name	RZ/A2M Pin	Note
1	VLED-	VLED-	-	
2	VLED+	VLED+	-	
3	GND	GND	-	
4	VDD	3V3D	-	
5	R0	LCD0_DATA0	F4	
6	R1	LCD0_DATA1	C1	
7	R2	LCD0_DATA2	D9	
8	R3	LCD0_DATA3	B8	
9	R4	LCD0_DATA4	A9	
10	R5	LCD0_DATA5	D11	
11	R6	LCD0_DATA6	B14	
12	R7	LCD0_DATA7	C14	
13	G0	LCD0_DATA8	D14	
14	G1	LCD0_DATA9	D15	
15	G2	LCD0_DATA10	B17	
16	G3	LCD0_DATA11	D16	
17	G4	LCD0_DATA12	C17	
18	G5	LCD0_DATA13	B18	
19	G6	LCD0_DATA14	A20	
20	G7	LCD0_DATA15	B19	
21	B0	LCD0_DATA16	B20	
22	B1	LCD0_DATA17	D17	
23	B2	LCD0_DATA18	C19	
24	B3	LCD0_DATA19	F22	
25	B4	LCD0_DATA20	G20	
26	B5	LCD0_DATA21	G21	
27	B6	LCD0_DATA22	H19	
28	B7	LCD0_DATA23	H21	
29	GND	GND	-	
30	PLCK	LCD0_CLK	K2	
31	DISP	LCD0_TCON0	J20	
32	HSYNC	LCD0_TCON1	J21	
33	VSYNC	LCD0_TCON2	L22	
34	DE	LCD0_TCON3	AA19	
35	NC	-	-	Not used
36	GND	GND	-	
37	XR	-	-	Not used
38	YD	-	-	Not used
39	XL	-	-	Not used
40	YU	-	-	Not used

4.7 CN9: LCD CAPACITIVE TOUCH

Figure 21. CN9 Front View

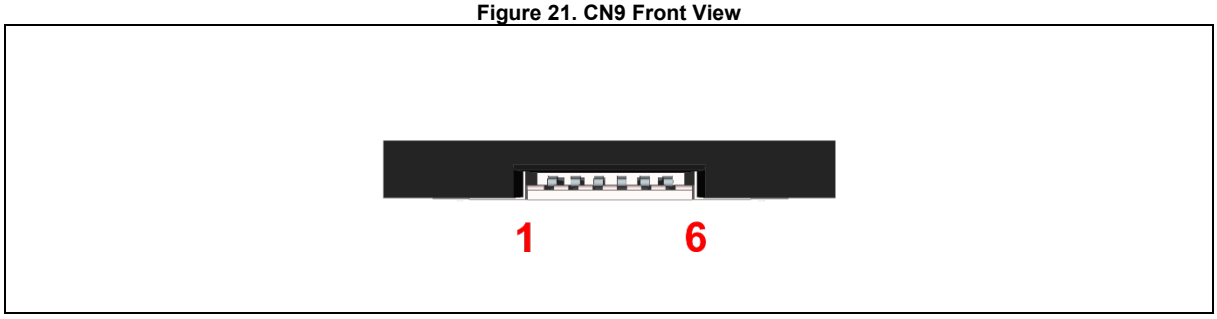


Table 42. CN8 Pin Assignment

CN9 Pin	Pin Description	Signal Name	RZ/A2M Pin	Note
1	SCL	RIIC3SCL	D20	
2	SDA	RIIC3SDA	C21	
3	VDD	3V3D	-	
4	RST	nRESET_SYS	-	
5	INT	TOUCH_IRQ1	AA22	
6	GND	GND	-	

4.8 CN10: 8 BIT VGA CAMERA MODULE

Figure 22. CN10 Front View

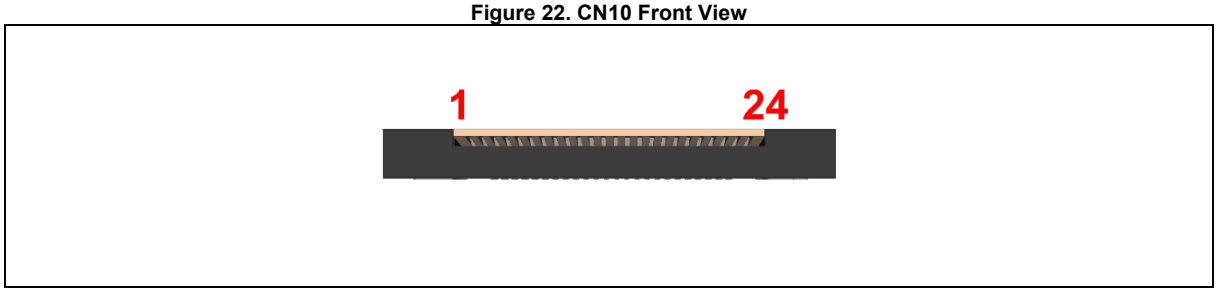


Table 43. CN10 Pin Assignment

CN10 Pin	Pin Description	Signal Name	RZ/A2M Pin	Note
1	SFIN	-	-	Pulled-down
2	AGND	GND	-	
3	SDA	RIIC3SDA	D20	SIOD
4	AVDD	GND	-	
5	SCL	RIIC3SCL	C21	SIOC
6	/RST	CAM_RST	P1	
7	VSYNC	VIO_VD	C9	
8	PWDN	CAM_PWR_DN	P2	
9	HSYNC	VIO_HD	B9	HREF
10	VCORE	-	-	100nF to GND
11	DVDD	3V3D	-	
12	Y9	VIO_D7	A19	
13	XCLK	-	-	27MHz osc.
14	Y8	VIO_D6	C16	
15	DGND	GND	-	
16	Y7	VIO_D5	B16	
17	PCLK	VIO_CLK	C8	
18	Y6	VIO_D4	A15	
19	Y2	VIO_D0	C10	
20	Y5	VIO_D3	A12	
21	Y3	VIO_D1	B10	
22	Y4	VIO_D2	A10	
23	Y1	-	-	Not used
24	Y0	-	-	Not used

4.9 CN11: MIPI-CSI2 CAMERA MODULE

Figure 23. CN11 Front View

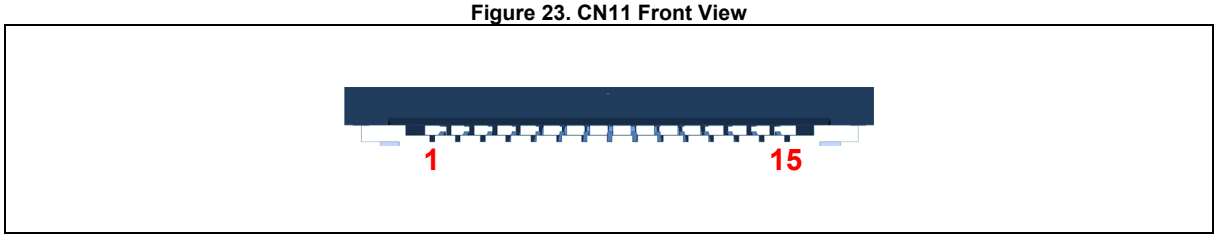


Table 44. CN11 Pin Assignment

CN11 Pin	Pin Description	Signal Name	RZ/A2M Pin	Note
1	GND	GND	-	
2	CSI_D0N	CSI_DATA0N	W2	
3	CSI_D0P	CSI_DATA0P	W1	
4	GND	GND	-	
5	CSI_D1N	CSI_DATA1N	Y2	
6	CSI_D1P	CSI_DATA1P	Y1	
7	GND	GND	-	
8	CSI_CLKN	CSI_CLKN	V2	
9	CSI_CLKP	CSI_CLKP	V1	
10	GND	GND	-	
11	EN	CAM_EN	M20	Pulled-up
12	NC	-	-	
13	SCL	RIIC3SCL	D20	
14	SDA	RIIC3SDA	C21	
15	VCC	3V3D	-	

4.10 CN12: 4-POLE AUDIO JACK

Figure 24. CN12 Mating Plug and Bottom View

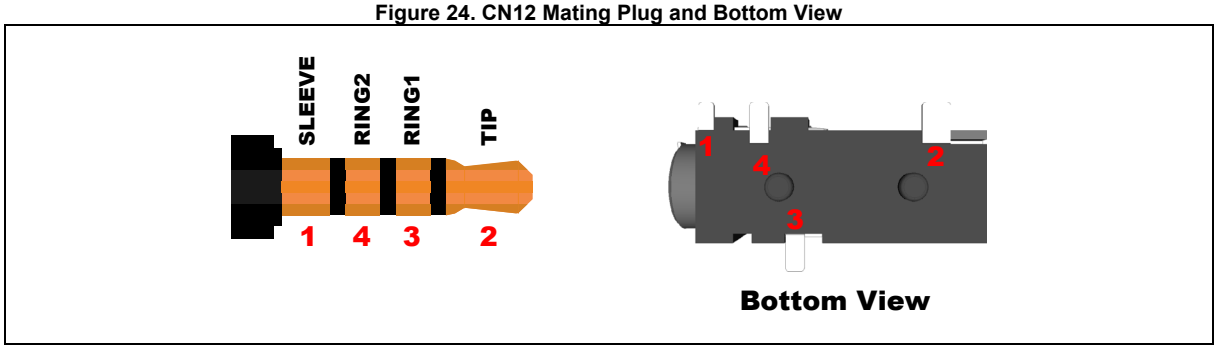


Table 45. CN12 Pin Assignment

CN12 Pin	Pin Description	Signal Name	U13 Pin	Note
1	SLEEVE	MIC	17	
2	TIP	LEFT	22	Single ended
3	RING1	RIGHT	19	Single ended
4	RING2	GND	GND	

4.11 CN13: EXPANSION CONNECTOR - MIKROBUS

Figure 25. CN13 Mikrobus Top view

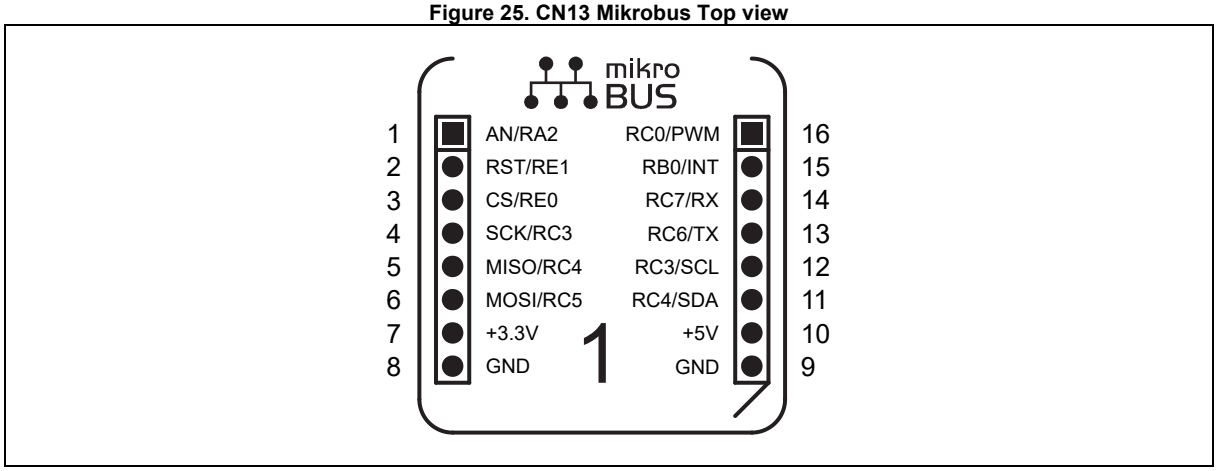


Table 46. CN13 Pin Assignment

CN13 Pin	Pin Description	Signal Name	RZ/A2M Pin	Function ID#	Note
1	AN/RA2	MIKROBUS_AN	Y21	Function 1	Multiplexed with POT
2	RST/RE1	MIKROBUS_RST	N21	GPIO	
3	CS/RE0	SSL20	AB17	Function 4	
4	SCK/RC3	RSPCK2	Y6	Function 3	
5	MISO/RC4	MISO2	W8	Function 4	
6	MOSI/RC5	MOSI2	AA6	Function 4	
7	+3.3V	3V3D	-	-	
8	GND	GND	-	-	
9	GND	GND	-	-	
10	+5V	5V_IN	-	-	
11	RC4/SDA	RIIC2SDA	E19	Function 1	
12	RC3/SCL	RIIC2SCL	D21	Function 1	
13	RC6/TX	TXD_MIKROBUS	AB7	Function 4	Multiplexed on JP2
14	RC7/RX	RXD_MIKROBUS	Y8	Function 4	Multiplexed on JP2
15	RB0/INT	MIKROBUS_IRQ6	U3	Function 6	
16	RC0/PWM	P6_6	M19	GPIO	

Table 47. Mikrobus Overview

Device Type	MFR[1] / MPN[2]	Package	Note
Mikrobus Connector	Wurth Electronics / 61300811821	2.54mm	CN13.1 & CN13.2[1]

Note 1: For manufacturing purposes CN13 is separated into 2 references CN13.1 and CN13.2

4.12 CN14/CN15: EXPANSION CONNECTORS – PMOD

Figure 26. PMOD Front View

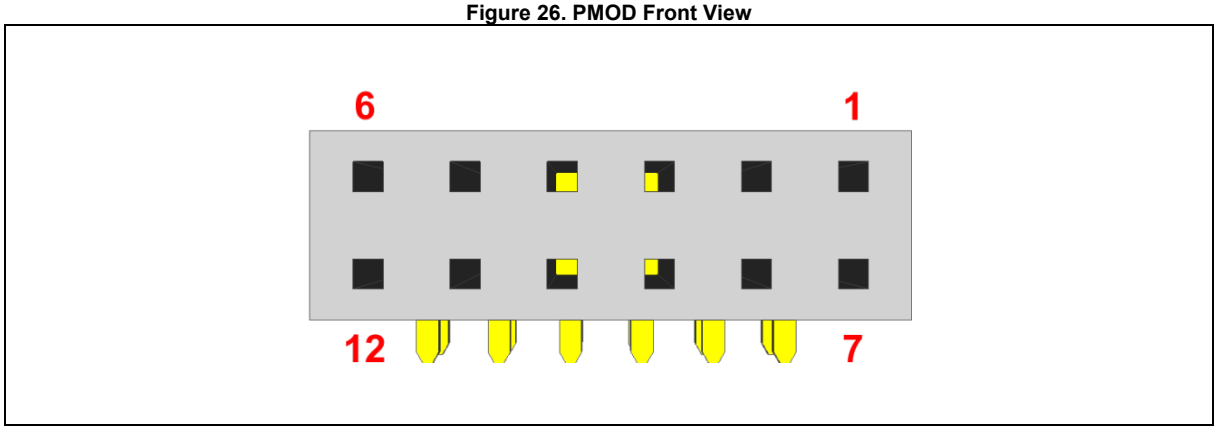


Table 48. CN14 Pin Assignment

CN14 Pin	Pin Description	Signal Name	RZ/A2M Pin	Function ID#	RZ/A2M Pin Description
1	CS	SSL00	N20	Function 3	PG_3 / SSL00
2	MOSI	MOSI0	K20	Function 3	PG_1 / MOSI0
3	MISO	MISO0	K22	Function 3	PG_2 / MISO0
4	SCK	RSPCK0	C18	Function 3	PG_0 / RSPCK0
5	GND	GND	-	-	-
6	VCC	3V3D	-	-	-
7	GPIO/INT	PMOD1_IRQ2	W20	Function 2	P5_6 / IRQ2
8	GPIO/RST	PMOD1_RST	AA8	GPIO	P4_4
9	GPIO/CS2	RIIC0SCL	F19	Function 1	PD_0 / RIIC0SCL
10	GPIO/CS3	RIIC0SDA	D22	Function 1	PD_1 / RIIC0SDA
11	GND	GND	-	-	-
12	VCC	3V3D	-	-	-

Table 49. CN15 Pin Assignment

CN15 Pin	Pin Description	Signal Name	RZ/A2M Pin	Function ID#	RZ/A2M Pin Description
1	CS	SSL10	AB3	Function 3	PG_7 / SSL10
2	MOSI	MOSI1	AB2	Function 3	PG_5 / MOSI1
3	MISO	MISO1	W4	Function 3	PG_6 / MISO1
4	SCK	RSPCK1	V3	Function 3	PG_4 / RSPCK1
5	GND	GND	-	-	-
6	VCC	3V3D	-	-	-
7	GPIO/INT	PMOD2_IRQ7	AA21	Function 2	P5_3 / IRQ7
8	GPIO/RST	PMOD2_RST	AA9	GPIO	P4_7
9	GPIO/CS2	RIIC1SCL	E20	Function 1	PD_2 / RIIC1SCL
10	GPIO/CS3	RIIC1SDA	C22	Function 1	PD_3 / RIIC1SDA
11	GND	GND	-	-	-
12	VCC	3V3D	-	-	-

4.13 CN16: +5VDC POWER JACK

Figure 27. CN16 Power Jack

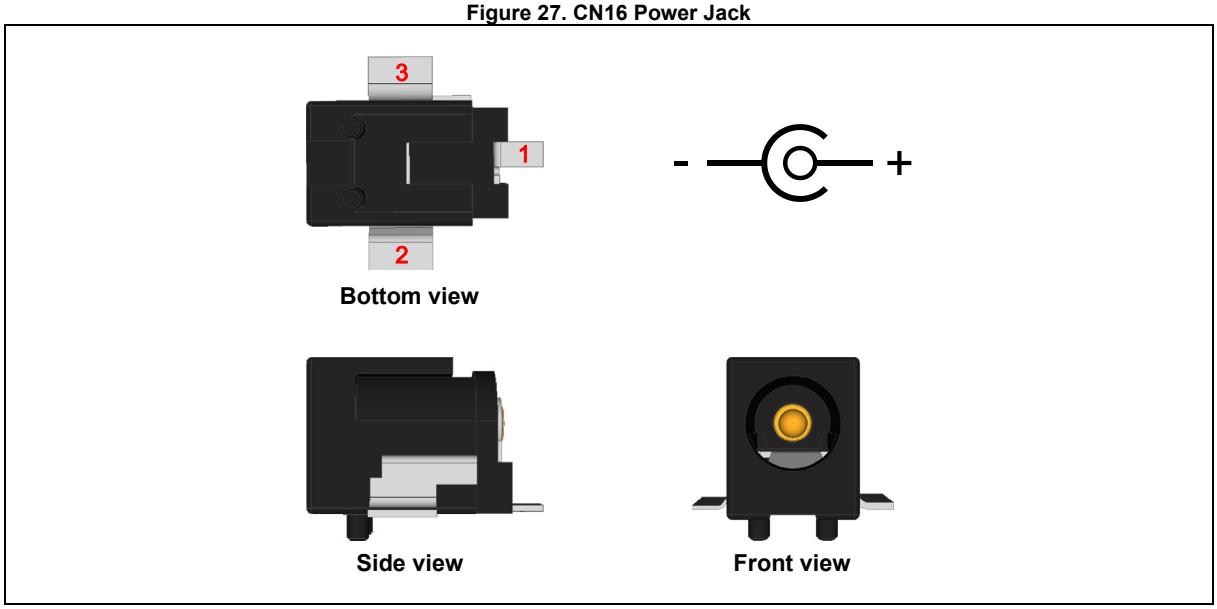


Table 50. CN16 Pin Assignment

CN14 Pin	Pin Description	Signal Name	Note
1	Center Pin	V_JACK	Strictly +5VDC
2	Outer Ring	GND	
3	Detect	-	Note used

5 OPERATING FUNCTIONS

5.1 SW4: BOOT AND CLOCK SELECT

SW4 DIP switch is used to select the RZ/A2M BOOT mode, the Clock Configuration and the Debug Setting. Figure 28 shows you how each pin is assigned to the RZ/A2M.

Figure 28. Boot & Clock Select switch Top View

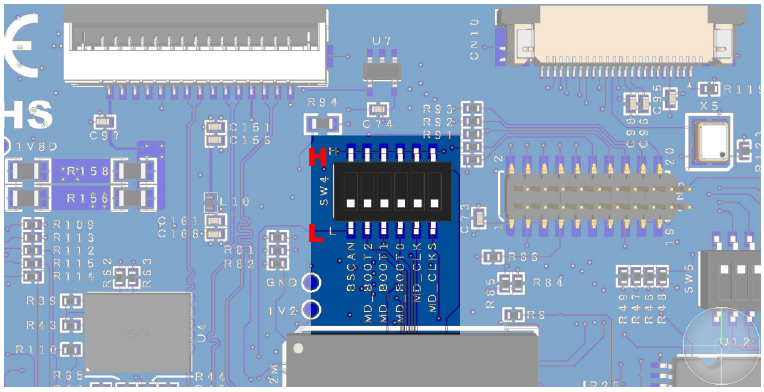


Table 51. SW4 Pin Assignment

SW4 Way	SW4 Pin	Signal Name	RZ/A2M Pin	Function ID#	RZ/A2M Pin Description
6	7-6	BSCANP	D2	DF[1]	BSCANP
5	8-5	MD_BOOT2	A11	DF[1]	PL_2 / MD_B00T2
4	9-4	MD_BOOT1	B11	DF[1]	PL_3 / MD_B00T1
3	10-3	MD_BOOT0	C11	DF[1]	PL_4 / MD_B00T0
2	11-2	MD CLK	B12	DF[1]	PL_1 / MD_CLK
1	12-1	MD_CLKS	C12	DF[1]	PL_0 / MD_CLKS

Table 52, Table 53, Table 54 and Table 55 shows you the possible configurations for each signal used for the choosing the Boot Mode.

Table 52. BSCANP Overview

BSCAN	FUNCTION
L	Normal operation (CoreSight debug mode)
H	Boundary-scan mode

Table 53. Boot Mode Selection

BOOT MODE	BSCAN	MD_ BOOT2	MD_ BOOT1	MD_ BOOT0	BOOT DEVICE
Boot Mode 0	L	L	L	L	Memory connected to the CS0 space (Bus width:16 bits)
Boot Mode 1	L	L	L	H	eSD
Boot Mode 2	L	L	H	L	eMMC
Boot Mode 3	L	L	H	H	Serial Flash on SPIBSC space, 3.3V (Default)
Boot Mode 4	L	H	L	L	OctaFlash on SPIBSC space, 1.8V
Boot Mode 5	L	H	L	H	HyperFlash on SPIBSC space, 1.8V
Boot Mode 6	L	H	H	L	OctaFlash on OctaFlash space, 1.8V
Boot Mode 7	L	H	H	H	HyperFlash on HyperFlash space, 1.8V (Secondary)

Table 54. MD_CLK Overview

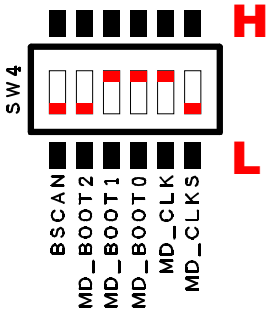
BSCAN	MD_CLK	FUNCTION
L	L	Sets EXTAL source range to “10 to 12 MHz”
L	H	Sets EXTAL source range to “20 to 24 MHz” (Default)

Table 55. MD_CLKS Overview

BSCAN	MD_CLKS	FUNCTION
L	L	SSCG Operation are OFF (Default)
L	H	SSCG Operation is ON

Table 56 shows you the default configuration of the **M13-RZ/A2M-EK** board.

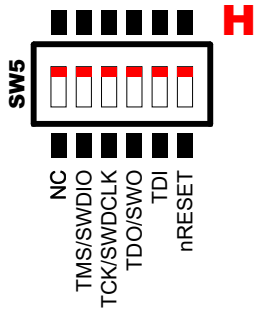
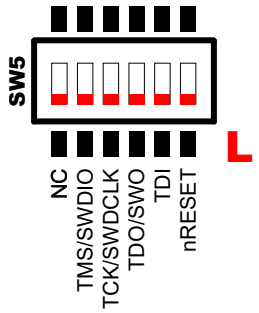
Table 56. SW4 Default Configuration

SW4 switch position	Description
	**Default configuration:** - CoreSight Debug Mode, - Boot Mode 3 (Serial Flash SPIBSC) - EXTAL range set to “20 to 24MHz” - SSCG Operation OFF

5.2 SW5: J-LINK OB DISCONNECTION SWITCH

Table 57 illustrate the setting of SW5. AS you can see, there are only 2 possible settings. Any other setting outside of the ones illustrated are prohibited.

Table 57. SW5 Settings

SW5 switch position	Description
	**J-LINK OB is used as the main Debugger: (Default)** All Switches from SW5 are in position “H”
	**An external probe is connected on CN5:** All Switches from SW5 are in position “L”

5.3 JP2: SCIFA CHANNEL 0 MULTIPLEXING

The JP2 Jumper is used to multiplex the SCIFA Channel 0 either to the Audio CODEC or to the Mikrobus connector. Figure 29 and Table 58 illustrate JP2 pin assignment.

Figure 29. JP2 Top View

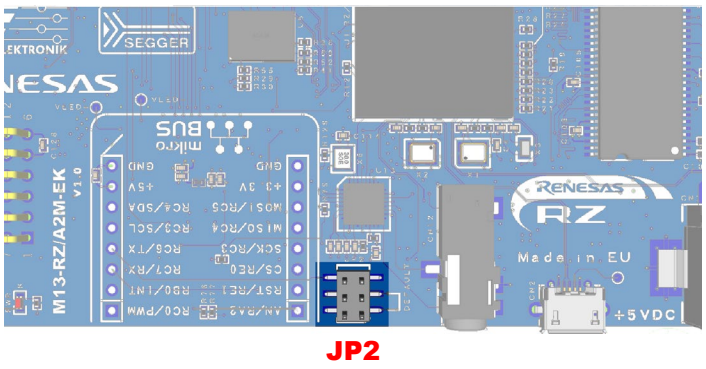
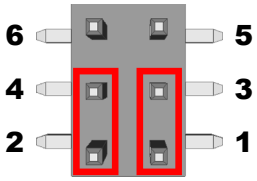
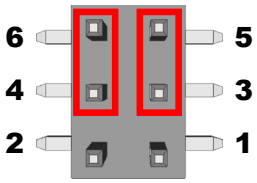


Table 58. JP2 Pin Assignment

JP2	Signal Name	RZ/A2M Pin	Function ID#	RZ/A2M Pin Description
1	SSITxD1	-	-	-
2	SSIRxD1	-	-	-
3	P4_2_TxD0	Y8	Function 1	P4_2 / TxD0
4	P4_1_RxD0	AB7	Function 1	P4_1 / RxD0
5	RXD_MIKROBUS	-	-	-
6	TXD_MIKROBUS	-	-	-

Table 59. JP2 Settings

View	Description
	**The SCIFA Channel 0 is guided to the Audio CODEC (Default)** Jumper is set on 1-3 Jumper is set on 2-4
	**The SCIFA Channel 0 is guided to the Mikrobus** Jumper is set on 3-5 Jumper is set on 4-6

5.4 P5_4 MULTIPLEXING

P5_4 is by default wired to SW2 via R78 as shown in Figure 30 and can be rewired to the Audio CODEC (U13) IRQ pin if needed as stated in Table 60.

Figure 30. P5_4 Multiplexing

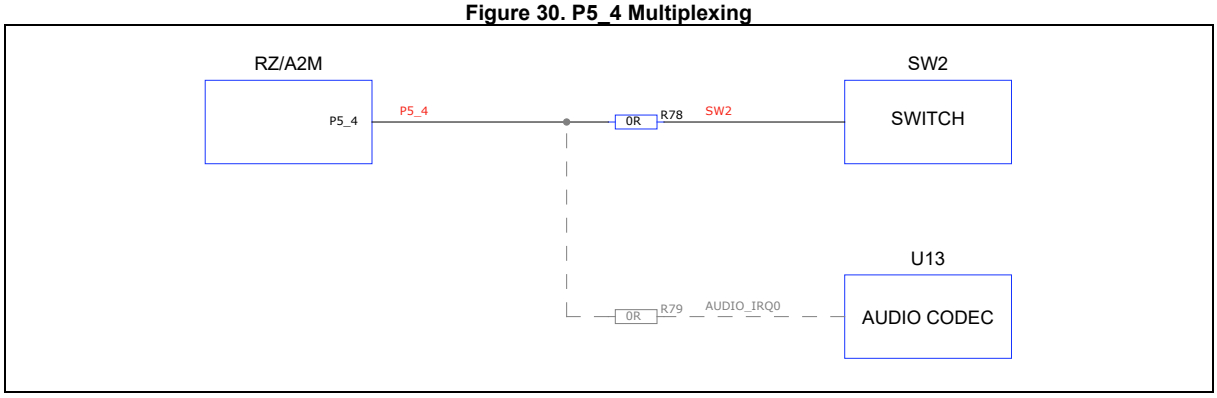


Table 60. P5_4 Setting

R78	R79	Multiplexing
Fitted	Not Fitted	SW2 (Default)
Not Fitted	Fitted	Audio Codec IRQ Pin U13.4
Fitted	Fitted	Forbidden

5.5 P5_7 MULTIPLEXING

P5_7 is by default wired to the 10K Potentiometer P1 via R76 as shown in Figure 31 and can be rewired to the Mikrobus' Analog Pin (CN13) as stated in Table 61.

Figure 31. P5_7 Multiplexing

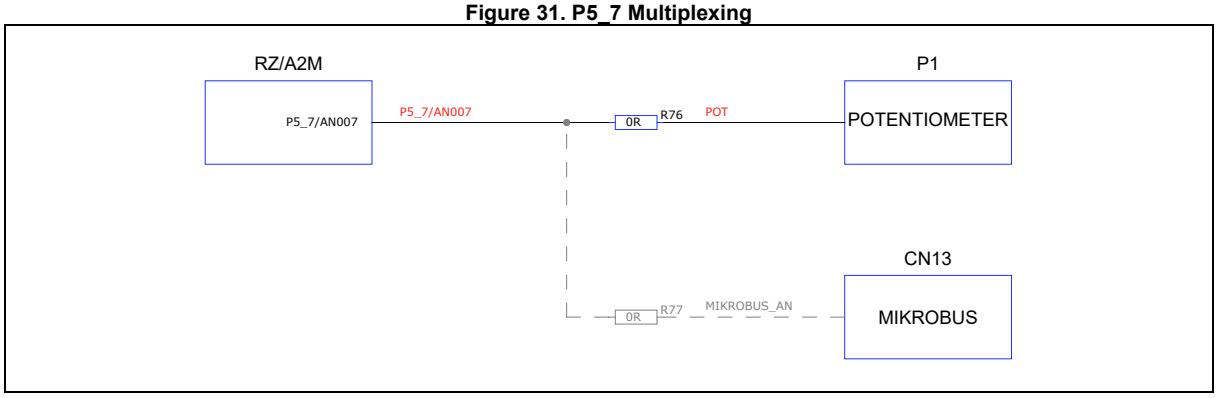


Table 61. P5_7 Setting

R76	R77	Multiplexing
Fitted	Not Fitted	Potentiometer P1 (Default)
Not Fitted	Fitted	Mikrobus Analog Pin CN13.1
Fitted	Fitted	Forbidden

6 RELATED DOCUMENTS

Please find below the links to other hardware related documents for this evaluation board.

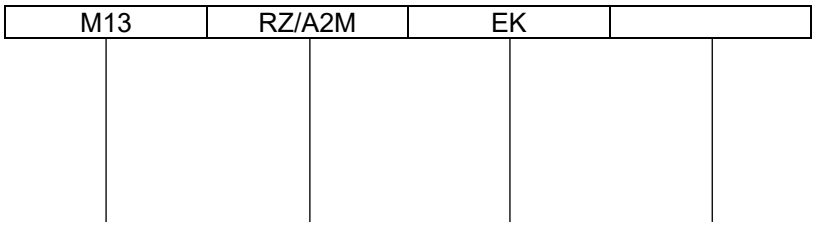
RZ/A2M Datasheet	/www.m13design.fr/download/pdf/M13design_M13-RZA2M-EK_Datasheet.pdf
RZ/A2M Schematic	www.m13design.fr/download/pdf/M13design_M13-RZA2M-EK_Schematic.pdf
RZ/A2M PCB layout	www.m13design.fr/download/pdf/M13design_M13-RZA2M-EK_PCB.pdf

Please refer to our product web page for any other information, here:
www.m13design.fr/products/M13-RZA2M-EK.html

7 ORDERING INFORMATION

Table 62. Ordering Information

Part Number	Variant Type	Eval Board	TD7740 camera	Raspberry Pi Camera	MIKROE-2046
M13-RZ/A2M-EK	Default	✓	✗	✗	✗
M13-RZ/A2M-EK-VGA	VGA Camera	✓	✓	✗	✗
M13-RZ/A2M-EK-MIPI	MIPI Camera	✓	✗	✓	✗
M13-RZ/A2M-EK-WIFI	Wi-Fi Module	✓	✗	✗	✓



M13design

MCU / MPU Type:
- RZ/A2M
- RA6M3
- Etc…

Evaluation Kit

Variant type:
- Blank: Default
- VGA: Include a VGA camera
- MIPI: Include a MIPI camera
- Wi-Fi: Include a Wi-Fi module for the Mikrobus Interface

8 TECHNOLOGY PARTNERS

Table 63. Hardware Technology Partners

Partners	Descriptions
RENESAS	Renesas Electronics Corporation delivers trusted embedded design innovation with complete semiconductor solutions that enable billions of connected, intelligent devices to enhance the way people work and live. A global leader in microcontrollers, analog, power, and SoC products, Renesas provides comprehensive solutions for a broa²d range of automotive, industrial, infrastructure, and IoT applications that help shape a limitless future.
WÜRTH ELEKTRONIK	Würth Elektronik eiSos is one of the leading manufacturers of electronic and electromechanical components in Europe. The product portfolio includes: EMC Components, EMC Filters, Capacitors, Inductors, RF Inductors and LTCC Components, Resistors, Quartz, Oscillators, Transformers, Components for Circuit Protection, Power Modules, LEDs, Connectors, Switches, High-Power Contacts, Assembly Technique, Wireless Connectivity and Sensors.
apmemory	AP Memory is a memory IC design company focusing on Low to Mid density RAM solutions, providing a full range of IoT RAM (low pin count QSPI/OPI PSRAM), ADMUX RAM (Cellular RAM), low power DRAM (LPDDR2/LPDDR3), as well as innovative solution for AI such as UHS OPI and more... Partnering with an advanced DRAM technology foundry, AP Memory provides world class performance, supply longevity, quality and cost, including high volume and customer oriented innovative and customized solutions, in both KGD and package form

Table 64. Software Technology Partners

Partners	Descriptions
cynetis embedded	Cynetis offers a range of innovative solutions for software design and development of embedded systems. Our portfolio includes ARM Cortex-M MCU and RTOS training classes, professional-grade middleware components (TCP/IP, SSL/TLS, SSH, GUI libraries, File Systems…) as well as world class embedded software tools (IDE, Debugger, JTAG/SWD & TRACE probes). For high-end embedded systems based on ARM Cortex-A MPUs, Cynetis promotes a broad range of System-on-Modules (SoM), Single Board Computers (SBC) and complete Human Machine Interfaces (HMI) targeting industrial, medical and vending machine markets. We also bring our expertise on both software (RTOS, Connectivity, Security, Embedded Linux) and hardware (ARM MCU/MPU) for a faster start of your embedded projects.
ORYX EMBEDDED	Oryx Embedded offers a complete range of networking solutions for embedded systems, making the Internet of Things a reality. Our portfolio includes professional-grade TCP/IP components as well as SSL/TLS & SSH encryption to make your communications safe and secure.
guiliani	Coming soon (Q3 / 2021) TES Electronic Solutions

9 REVISION HISTORY

Table 65. Revision Table

Revision	Date	Revision content
V1.0	03 Nov. 20	Initial release.
V1.0.1	04 Mar. 21	• Updated PMOD information to match schematic - PMOD LEFT changed to PMOD1 - PMOD RIGHT changed to PMOD2
V1.0.2	06 Apr. 21	• Replaced the HyperBus device with a OctaRAM device - Updated the section 1.2.Features - Updated the section 1.3.Memory mapping - Updated the section 2.1.Hardware block diagram - Changed section 3.2.2 to OctaRAM • Added section 7.Ordering information • Updated the links in section 6.Related documents • Updated Table 63 with AP Memory details • Updated Table 64 with TES Electronic Solutions / Guiliani

Disclaimer

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www.m13design.fr/contact/